A Dual Core Source/Drain GAA FinFET

Un FinFET GAA de fuente/drenaje de doble núcleo

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Keywords

FinFET; Gate-all-Around; Dual Core; Interface Traps; Ribbon FET.

Abstract

The emergence of fin-shaped field effect transistors (FinFETs) was governed by the requirement of the VLSI industry to include more functionalities per unit chip area. Enhanced gate control in a FinFET due to a surrounding gate architecture built on the fundamental geometry of a MOSFET made them highly compatible to the existing CMOS circuit applications. The announcement of a vertically stacked multiple FinFET structure named as Ribbon-FET by Intel Corporation in 2021 motivates the work presented in this article. This article proposes a dual core source-drain gate-all-around FinFET, and evaluates its performance in terms of variation in core doping concentrations through technology computer aided design (TCAD) simulations. The advantage of having a dual core in source and drain regions is the opportunity to tune the performance metrics of the device by altering the doping concentration in the outer, and inner cores. The response of the optimized architecture to presence of acceptor-like, and donor-like traps in oxide/ channel interface is presented. The acceptor-like traps affect the characteristics in its on-state, whereas the donor-like traps influence the off-state of the device. DIBL reduces with the introduction of interface traps.

Palabras clave

FinFET; Puerta todo alrededor; Doble núcleo; trampas de interfaz; Ribbon FET.

Resumen

La aparición de transistores de efecto de campo en forma de aleta (FinFET) se rigió por el requisito de la industria VLSI de incluir más funcionalidades por unidad de área de chip. El control de puerta mejorado en un FinFET debido a una arquitectura de puerta circundante construida sobre la geometría fundamental de un MOSFET los hizo altamente compatibles con las aplicaciones de circuitos CMOS existentes. El anuncio de una estructura FinFET múltiple apilada verticalmente denominada Ribbon-FET por Intel Corporation en 2021 motiva el trabajo presentado en este artículo. Este artículo propone un FinFET completo de puerta de drenaje de fuente de doble núcleo y evalúa su rendimiento en términos de variación en las concentraciones de dopaje del núcleo a través de simulaciones de tecnología de diseño asistido por computadora (TCAD). La ventaja de tener un núcleo doble en las regiones de origen y drenaje es la oportunidad de ajustar las métricas de rendimiento del dispositivo alterando la concentración de dopaje en los núcleos externo e interno. Se presenta la respuesta de la arquitectura optimizada a la presencia de trampas de tipo aceptor y de tipo donante en la interfaz óxido/canal. Las trampas de tipo aceptor afectan las características en su estado activado, mientras que las trampas de tipo donante influyen en el estado desactivado del dispositivo. DIBL se reduce con la introducción de trampas de interfaz.

Introduction

The improved gate control on channel by transforming the body of planar metal oxide semiconductor field-effect transistors (MOSFETs) into a fin-shaped geometry has made FinFETs one of the quickest architectures to have a research-to-market translation [1]. The orientation of the semiconductor device industry towards ribbon-FET architectures or multi-level vertically stacked gate-all-around (GAA) structures to address efficient power management has created

the need for evaluating architectures with more control parameters [2]. This article proposes a dual core (DC) GAA FinFET with dual doping concentration in its source, and drain regions, and examines it for variation in doping concentration, and presence of interface traps through technology computer-aided design (TCAD) simulations.

Device architecture and simulation set-up

The schematic of the DC GAA FinFET is shown in Fig. 1 (a)-(c), where the source, and drain regions have dual cores (outer core doping: OC, inner core doping: IC), and the channel region is a solo core structure with a doping concentration of $10^{17} cm^{-3}$. Such a geometry offers the option to modulate the electrical characteristics of the proposed architecture through change in doping concentrations. Calibrated simulations have been carried out on Sentaurus TCAD tool (Synopsys Inc.) [3] in accordance with the parameters as mentioned in the article, [4].

(a)   (b)   (c)
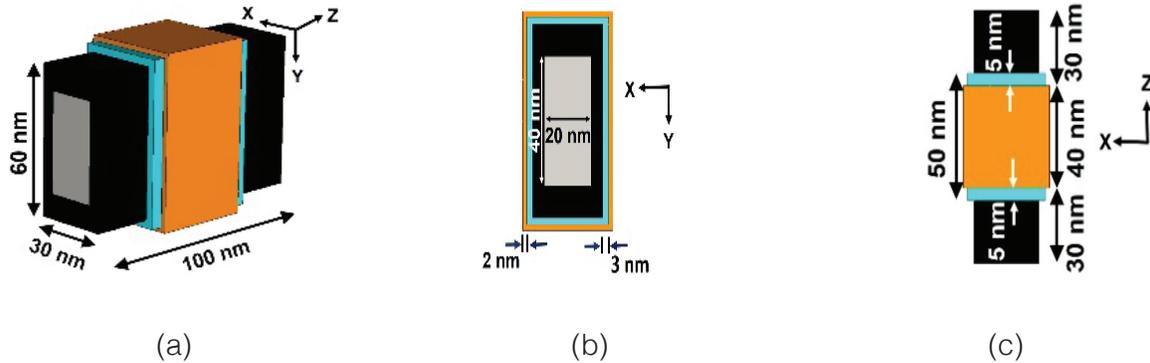
Figure 1. (a) 3D view; (b) Front view; (c) Top view of the DCGAA FinFET.

Results and discussion

The effect of variation in dual core doping concentration on transfer characteristics of the proposed device with SiO_2 as a gate oxide (GOx) is shown in Fig. 2 (a). The presence of bandgap narrowing model (BGN) slightly decreases the drain current as shown in the inset due to the change in energy bandgap in regions of high doping. Therefore, the barrier height increases for carriers in source/ channel junction as evident from the conduction band edge profile in Fig. 2 (b), plotted along the source-channel-drain position (z-axis) at $x = W/2$, $y = H/2$ (W: fin width, H: fin height) at $V_{GS} = 0.1$ V. As evident from Fig. 2 (a), and Table 1, OC = IC = 10^{19}cm^{-3} offer the highest on-state current I_{ON} , yet, it offers a lower switching current ratio (I_{ON}/ I_{OFF}). On the contrary, OC = IC = 10^{18} cm^{3} offer the best off-state current (I_{OFF}), threshold voltage (V_{TH}), and subthreshold swing (SS). A further insight into the absolute electric field profiles along the z-axis at $x = W/2$, $y = H/2$ for all the four cases of doping concentrations in Fig. 2 (c) in on-state shows the maximum peak for OC = IC = 10^{19} cm^{3}, and the minimum peak for OC = IC = 10^{18} cm^{3}.

(a)

(b)

(c)
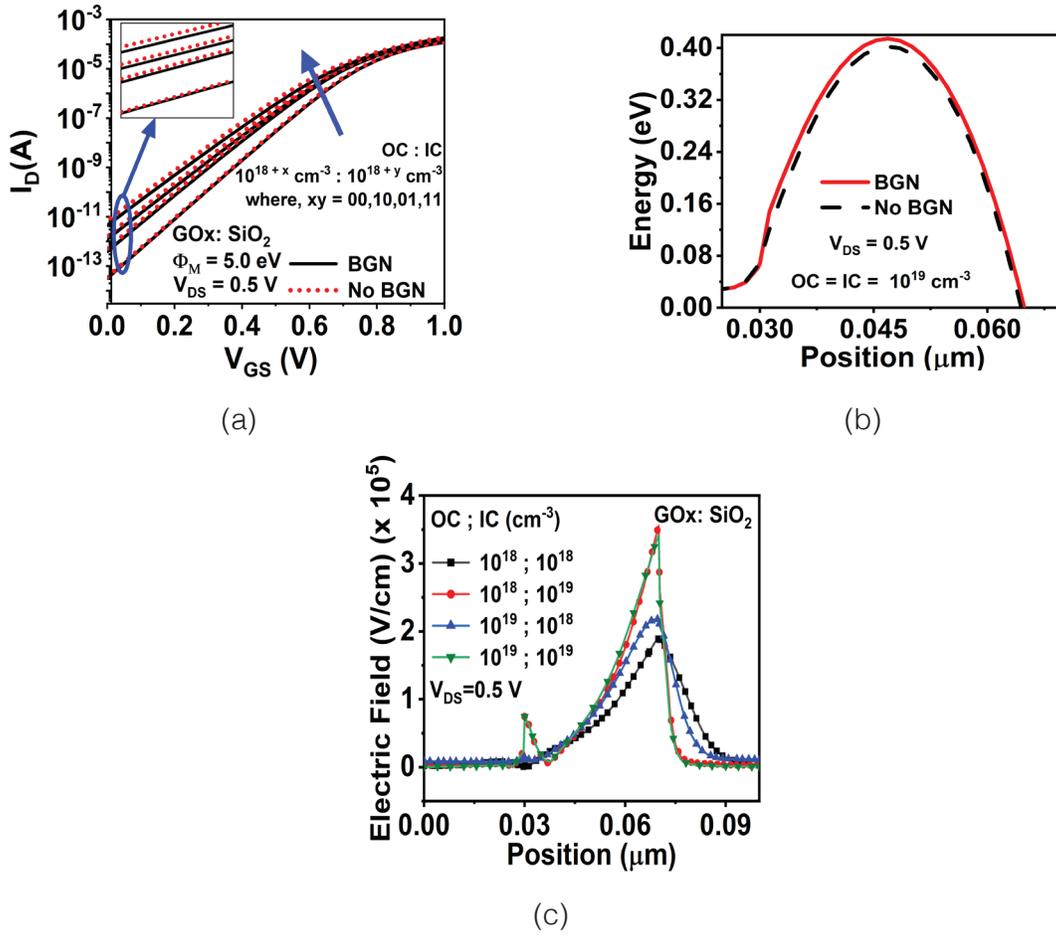
Figure 2. (a) Transfer characteristics of DC GAA FinFET for different outer core (OC), and inner core (IC) doping concentrations with and without bandgap narrowing effects; (b) Conduction band energy with and without BGN in the channel along z-axis at $x = W/2$, $y = H/2$ $V_{GS} = 0.1V$; (c) Absolute electric field profiles along z-axis at $x = W/2$, $y = H/2$.

Table 1. Electrical characteristics of DC GAA FinFET for different core doping concentrations without BGN [Fig. 2 (a)]

Outer Core Doping (cm^{-3})	Inner Core Doping (cm^{-3})	I_{ON} (μA)	I_{OFF} (ρA)	I_{ON}/I_{OFF} (x 10^7)	V_{TH} (V)	Subthreshold Swing (mV/dec)
10^{18}	10^{18}	118.833	0.031	378.6	0.777	84.123
10^{18}	10^{19}	154.151	1.200	12.83	0.778	96.654
10^{19}	10^{18}	165.869	0.385	43.02	0.791	87.499
10^{19}	10^{19}	179.678	4.476	4.013	0.781	99.600

To consider an optimized set of electrical characteristics with priority on I_{ON}, and I$_{ON}$/I$_{OFF}$, the architecture with $OC = 10^{19}$ cm^3, and $IC = 10^{18}$ cm^3 is considered for further observations, taking HfO$_2$ as gate oxide (GOx). Figure 3 (a) compares the transfer characteristics of the optimized architecture in the absence, and presence of trap states (acceptor-like traps, and donor-like traps) at the gate-oxide/ channel interface. The trap distribution is considered to be Gaussian, and defined in the TCAD tool as,

$$D_{GAU} = N_0 exp \left| \frac{(E - E_0)^2}{2E_S^2} \right|$$

(1)

where, $N_0 = 10^{13} \, cm^2$, $E_0 = 0.55 \, eV$ from valence band edge, $E_S = 0.1 \, eV$ [5].

(a)

(b)

(c)
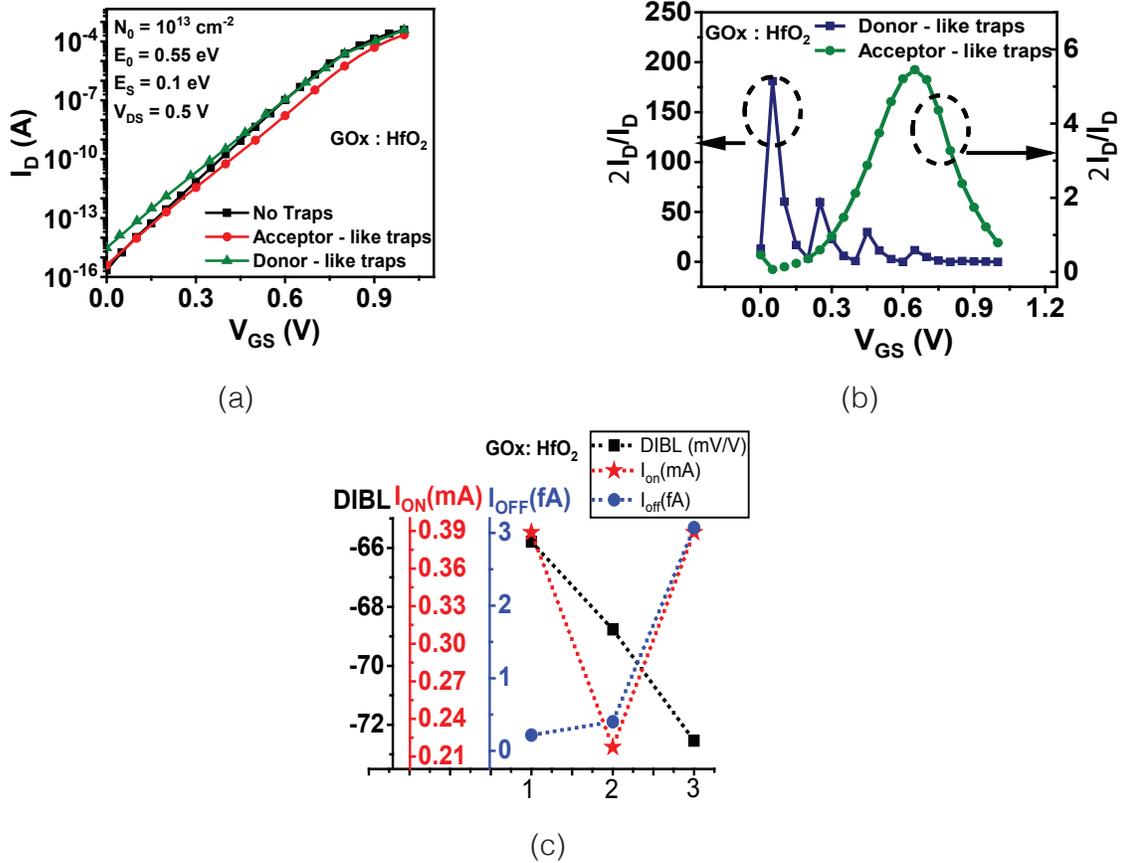
Figure 3. (a) Transfer characteristics of DC GAA FinFET for optimized doping concentrations in presence, and absence of oxide/channel interface traps having Gaussian distribution, peaked at 0.55 eV, and standard deviation of 0.1 eV; (b) Trap sensitivity for the transfer characteristics in (a); (c) Comparison plots of DIBL, I_{OFF}, and I_{ON} for no traps (Sl. 1), acceptor-like traps (Sl. 2), and donor-like traps (Sl. 3)

It is observed that the transfer characteristics in absence of traps overlaps with the characteristics for acceptor-like traps in off-state, and overlaps with the characteristics for donor-like traps in on-state. The comparison becomes more prominent when the trap sensitivity is plotted in Fig. 3 (b) in terms of $\Delta I_D/I_D$ where I_D is the drain current, taking the case for no traps as a reference [5]. The case for donor-like traps exhibits maximum peak in the low-V_{GS} region close to off-state, whereas for acceptor-like traps, the peak is exhibited in the mid-V_{GS} region in the on-state. Figure 3 (c) presents a multi-YYY plot for drain induced barrier lowering (DIBL), I_{OFF}, and I_{ON} for three cases: 1 (no traps), 2 (acceptor-like traps), and 3 (donor-like traps). The DIBL, measured using constant current method at $I_D = 0.1 \, \mu A$ decreases as interface traps are introduced, which indicates that the trapping of carriers close to the interface is dominant enough to reduce the ΔV_{TH} difference at lower, and higher V_{DS}.

With reference to the inference from Fig. 3 (b), electrostatic potential profiles are plotted for acceptor-like traps (on-state, $V_{GS} = 0.9V$), and donor-like traps (off-state, $V_{GS} = 0.0V$) in Fig. 4 (a) and Fig. 4 (b) by comparing with corresponding profiles for no traps at respective V_{GS}, showing the region(s) of influence where the variation is observed.
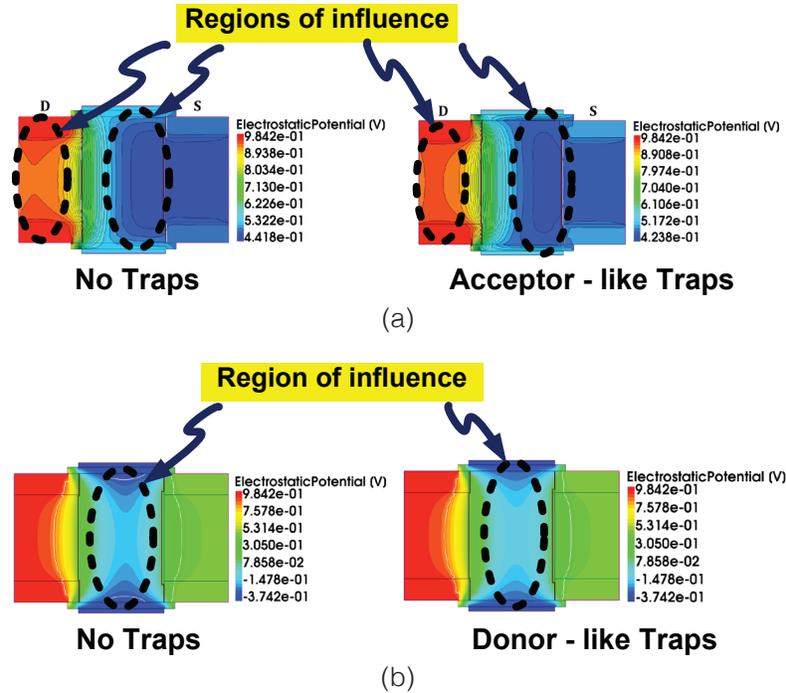
Figure 4. Electrostatic potentials along z-axis at $x = w/2$ for (a) acceptor-like traps at $V_{GS} = 0.9V$, and (b) donor-like traps at $V_{GS} = 0.0V$ by comparing with corresponding profiles for no traps in respective V_{GS}.

Conclusion

This article proposed a geometry of a dual core source/ drain FinFET, and reported its performance in absence, and presence of interface traps. The conclusions of the article can be summed up as follows.

- Modulation of electrical parameters is possible by tuning the doping concentrations in the two cores.

- Donor-like interface traps are dominant in off-state, whereas acceptor-like interface traps are dominant in on-state. The parameter, interface trap sensitivity, reveals this nature.

- DIBL reduces with the introduction of interface traps.

Acknowledgment

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ABSTRACT

This article proposes a dual core source-drain gate-all-around FinFET, and evaluates its performance in terms of variation in core doping concentrations through technology computer aided design (TCAD) simulations. The response of the optimized architecture to presence of acceptor-like, and donor-like traps in oxide/ channel interface is presented. The acceptor-like traps affect the characteristics in its on-state, whereas the donor-like traps influence the off-state of the device.

INTRODUCTION

FinFETs are one of the fastest architectures to go from research to market. They have increased gate control on channel by converting the body of planar MOSFETs into fin-shaped geometry[1]. To solve effective power management, the semiconductor device industry has shifted its focus toward ribbon-FET architectures or multi-level vertically stacked gate-all-around (GAA) structures. Intel introduces vertical stacking of GAA FinFETs (named as Ribbon FET) in 2021[2].

DEVICE ARCHITECTURE AND SIMULATION SET-UP

The schematic of the DC GAA FinFET is shown in Fig. 1 (a)-(c), where the source, and drain regions have dual cores (outer core doping: OC, inner core doping: IC), and the channel region is a solo core structure with a doping concentration of $10^{17} cm^{-3}$. Such a geometry offers the option to modulate the electrical characteristics of the proposed architecture through change in doping. Calibrated simulations have been carried out on Sentaurus TCAD tool (Synopsys Inc.) in accordance with the parameters as mentioned in [3][4].
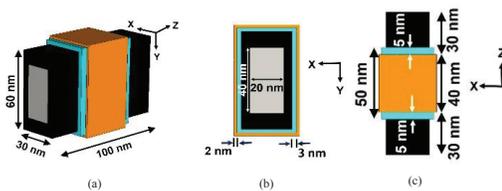
Figure 1: (a) 3D view; **(b)** Front view; **(c)** Top view of Dual Core (DC) GAA FinFET

RESULTS AND DISCUSSION

Table 1. Electrical characteristics of DC GAA FinFET for different core doping concentrations without BGN [Figure 2]

Outer Core Doping (cm^{-3})	Inner Core Doping (cm^{-3})	I_{ON} (μA)	I_{OFF} (pA)	I_{ON}/I_{OFF} ($\times 10^7$)	V_{TH} (V)	Subthreshold Swing (mV/dec)
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10^{19}	10^{18}	165.869	0.385	43.02	0.791	87.499
10^{19}	10^{19}	179.678	4.476	4.013	0.781	99.600

Figure 2

❖ As evident from Figure 1 (d), and Table 1, $OC = IC = 10^{19} cm^{-3}$ offer the highest on-state current (I_{ON}), yet, it offers a lower switching current ratio (I_{ON}/I_{OFF}).

❖ $OC = IC = 10^{18} cm^{-3}$ offer the best off-state current (I_{OFF}), threshold voltage (V_{TH}), and subthreshold swing (SS).
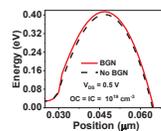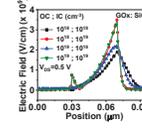
Figure 3

Figure 4

❖The presence of bandgap narrowing model (BGN) slightly decreases the drain current as shown in the inset due to the change in energy bandgap in regions of high doping[Figure 3].

❖ The absolute electric field profiles along the z-axis at $x = W/2$, $y = H/2$ for all the four cases of doping concentrations in on-state shows in Figure 4.
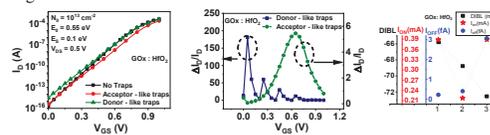
Figure 5

Figure 6

Figure 7
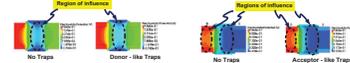
Figure 8

❖ The transfer characteristic shown in Figure 5 for no traps overlaps with the characteristic for acceptor-like traps in off-state, and overlaps with the characteristic for donor-like traps in on-state[5].

❖ Donor-like traps exhibits maximum peak in the low-V_{GS} region close to off-state[Figure 6].

❖ Acceptor-like traps, the peak is exhibited in the mid-V_{GS} region in the on-state [Figure 6].

❖ The DIBL, measured using constant current method at $I_D = 0.1\ \mu A$ decreases as interface traps are introduced [Figure 7].

❖ Indicates that the trapping of carriers close to the interface is dominant enough to reduce the ΔV_{TH} difference at lower, and higher V_{DS}.

CONCLUSION

❖Modulation of electrical parameters is possible by tuning the doping concentrations in the two cores.

❖Donor-like interface traps are dominant in off-state, whereas acceptor-like interface traps are dominant in on-state.

❖DIBL reduces with the introduction of interface traps.

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