An Elitist Non-Dominated Multi-Objective Genetic Algorithm Based Temperature Aware Circuit Synthesis

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Received 20 September 2019 | Accepted 13 February 2020 | Published 3 July 2020

Abstract

At sub-nanometre technology, temperature is one of the important design parameters to be taken care of during the target implementation for the circuit for its long term and reliable operation. High device package density leads to high power density that generates high temperatures. The temperature of a chip is directly proportional to the power density of the chip. So, the power density of a chip can be minimized to reduce the possibility of the high temperature generation. Temperature minimization approaches are generally addressed at the physical design level but it incurs high cooling cost. To reduce the cooling cost, the temperature minimization approaches can be addressed at the logic level. In this work, the Non-Dominated Sorting Genetic Algorithm-II (NSGA-II) based multi-objective heuristic approach is proposed to select the efficient input variable polarity of Mixed Polarity Reed-Muller (MPRM) expansion for simultaneous optimization of area, power, and temperature. A Pareto optimal solution set is obtained from the vast solution set of 3n ('n' is the number of input variables) different polarities of MPRM. Tabular technique is used for input polarity conversion from Sum-of-Product (SOP) form to MPRM form. Finally, using CADENCE and HotSpot tool absolute temperature, silicon area and power consumption of the synthesized circuits are calculated and are reported. The proposed algorithm saves around 76.20% silicon area, 29.09% power dissipation and reduces 17.06% peak temperature in comparison with the reported values in the literature.

Keywords

Thermal Aware, Mixed Polarity Reed-muller, Non-Dominated Sorting Genetic Algorithm-II, Tabular Technique.

DOI: 10.9781/ijimai.2020.07.003

I. Introduction

PARAMETERS such as area, power, and delay of highly complex logic circuits used in the field of digital systems can be appropriately optimized by utilizing AND-XOR based circuits rather than AND-OR based Boolean function [1]-[2]. Besides, XOR-based circuits are well suited for testability [3]-[4] and easily mapped into the Field Programmable Gate Arrays (FPGAs). Minimization of AND-XOR nodes (area count) is possible by sharing the sub-functions/ product terms within the multi-output functions. With the reduction of node count, the signal transitions among the sub-function get reduced. 'Espresso,' the two-level AND-OR minimizer was developed to eliminate redundant literals from canonical form using unite function decomposition [5]. Low power approaches are established by searching a suitable input variable polarity for maximum sharing of internal nodes to reduce the switching activity of a Boolean function [6]-[8]. There are several sub-classes of AND-XOR circuit synthesis which are of interest. The most general 2-level AND-XOR form is EXOR Sum-Of-Product (ESOP). Due to its non-canonical nature, ESOPs are very hard for optimization. It is observed that any Boolean function can be represented in modulo-2 AND-XOR based algebraic expressions. These expressions are elaborated with the help of Davio functions [9], and are termed as Reed-Muller (RM) expansions. A Boolean function represented in RM form is unique and canonical in nature, consumes less area, reduces power dissipation, and is in readily testable form [4]-[6], [8]. Depending on application-specific advantages, RM circuits are represented in the Positive Polarity Reed-Muller (PPRM) expansion, Fixed Polarity Reed-Muller (FPRM) expansion and Mixed Polarity Reed-Muller (MPRM) expansion. A thorough search on literature review has shown that optimization of MPRM is superior over the FPRM expansions on circuit performance regarding the area, switching activity (dynamic power) and/or delay [6]-[8], [10]-[11]. A fast minimization algorithm (FMA) using the binary differential evolution (BDE) method to minimize the FPRM product term is proposed in [12]. A comparative study of proposed FMA with the genetic algorithm (GA) and simulated annealing genetic algorithm (SAGA) is also reported. An incompletely specified FPRM (ISFPRM) acquisition algorithm is proposed by He et al. in [13]. The authors proposed a chromosome conversion technique to convert zero polarity ISFPRM to the FPRM for power reduction. A hybrid simulated annealing (SA) and discrete particle swarm optimization (DPSO) based area optimization approach is proposed in [14]. Authors in [8], considered the NSGA-II algorithm to find an optimal polarity for power and area optimization of MPRM network. Authors in [8] proposed a chromosome encoding method based on ternary input polarity and binary don't care allocation. By exploiting the don't care condition, authors in [15] proposed a delay optimization approach for MPRM based logic. In [15], the authors minimized the weighted

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path length using the Huffman tree construction algorithm. A shared mixed polarity RM (SMPRM) network is proposed using weighted search GA (WSGA) in [16] to find the optimal polarity based on area, power, and temperature. The trade-off analysis is also reported among the area, power, and temperature. But it is very difficult to find the optimum polarity in WSGA as one parameter may dominate the other. Other than [16], none of the articles have considered temperature as one of the cost metric for RM network synthesis. But consideration of temperature as a cost metric is very much essential because, ICs need to operate within a stipulated temperature zone prescribed by the manufacturers. The commercial devices and industrial devices are operating within the temperature zone of (0 °C to 70 °C) and (-40 °C to 85 °C) respectively, which are much lower than the aerospace and military devices operating zone (-55 °C to 125 °C) [17]-[18]. Due to aggressive device scaling and package density, most of the integrated circuits (ICs) are burnt just because of over-heating. Overheating is build-up due to excessive power density generation within the chip for the inclusion of a vast number of complex functionality within a small silicon area. So far most of the researchers paid attention to physical design domain for temperature minimization [19]-[20], but the cooling solutions are rising at $ 1-3 or more per watt of power dissipation [21]. The cooling cost of high-performance processor increases exponentially with the growth of power density. So, design-time thermal-aware techniques can be used to improve the power and thermal characteristics of integrated circuits. Few works report temperature minimization by reducing the power density at logic synthesis level [22]-[26]. The power density finds a direct relation with temperature generation within a chip by the following expression [27].

$$T_{chip} = T_{amb} + R_{th} \cdot \left[\frac{P_T}{A_T} \right] \tag{1}$$

In equation (1), T_{chip} and T_{amb} are the average chip temperature and ambient temperature respectively. Where, R_{th} is the summative equivalent thermal resistance of the substrate (Si) layer, package, and heat sink (m^2 °C/W). Total power dissipation is represented by P_T (in W). And A_T (in m^2) referred as total silicon core area of the chip. This area does not include the package area, but it consists of all cell area and routing area of Silicon chip. Earlier researchers ignore the thermal issues in higher levels (logic synthesis and circuit design) of very-large-scale integration (VLSI) design synthesis. In [28], Shang and Dick reported that rise in chip temperature set back reliability, performance, cost and power consumption. It is reported in [28] that 30% cost of IC packaging is contributed by cooling arrangement. The temperature determining parameter inclusion in logic synthesis level may reduce the cooling cost.

An exact or exhaustive search method can be used for small-sized circuits, but this strategy is not feasible for middle or large-sized circuits. The problem of determination of exact input variable polarity for getting minimum cost is a non-deterministic polynomial-time hard (NP-hard) problem. No known algorithm can solve this problem in polynomial time. Non-exhaustive or heuristic search approaches have been introduced to solve such NP-hard problems. Detail of NP-hard problems can be found in [29]. The proposed work presents a fast converging heuristic technique called Non-Dominated Sorting based Genetic Algorithm-II (NSGA-II) for the thermal-aware problem. Compared to existing optimization approaches, the contributions of the proposed approach are as follows:

- The thermal-aware AND-XOR logic synthesis is done suitably using MPRM expansion methodology.
- NSGA-II is used to get the optimum solution in terms of area, power, and power density for MPRM circuits. Parameters of the NSGA-II algorithm are tuned suitably to get the optimum solution.
- The simulation result of the proposed approach is reported by calculating the absolute temperature, total power consumption, and silicon area. 'HotSpot' tool [30] is used to report the absolute temperature. Cadence 'Innovus' tool [31] is used to report the total power consumption (dynamic and leakage) and silicon area at 45nm technology.

In the proposed approach, we considered the ternary input variable polarity for chromosome encoding and then modified the NSGA-II approach at crossover and mutation level to find the better offspring. Parent chromosomes for crossover and mutation are chosen from the elite group or entire population based on threshold value. Two-point crossover methodologies are used to generate the offspring chromosomes. Random bit positions are chosen to increase the mutation diversity within the offspring. In the proposed work, power density is considered as a cost metric to reduce the thermal effect in MPRM network. Finally, Electronic Design Automation tools (Cadence and HotSpot) are used for actual area, power and temperature calculation.

The rest of the paper is organized as follows: Section II demonstrates the motivation and basic terminologies used in RM expansion. Section III presents the Thermal-aware mixed polarity problem formulation using tabular technique approach. NSGA-II based thermal-aware realization is described in section IV. Section V details the results, and finally, section VI draws the conclusion.

II. Reed-Muller Preliminaries and Motivation

A. Reed-Muller Expansion

Any n-input m-output Boolean function can be represented canonically as AND-OR based Sum-Of-Product (SOP) form. The SOPs are expanded with 2^n different product terms as shown below:

$$f(x_n, \ldots\ldots, x_1) = \sum_{i=1}^{2^n} p_i . m_i \tag{2}$$

Where 'm_i' represents the minterms and $p_i \in \{0, 1\}$ represents the absence or presence of minterms. Suffix 'i' accounts for the number of terms which varies from 1 to 2^n. If all the input variables are used to represent the minterms of an expression, then it is said to be Canonical Sum-Of-Product (CSOP). In CSOP logic function all OR gates can be replaced with XOR gates and provides ExOR Sum-Of-Product (ESOP) function. The ESOP form can be represented as:

$$f(x_n, \ldots\ldots, x_1) = \oplus \sum_{i=1}^{2^n} p_i . m_i \tag{3}$$

Here, $\oplus$ represent the ExOR operation. The expanded ESOP form can be written as:

$$f(x_n, \ldots\ldots, x_1) = p_1 \overline{x_n} \ldots \overline{x_2}\,\overline{x_1} \oplus p_2 \overline{x_n} \ldots \overline{x_2} x_1 \oplus \ldots \oplus p_{2^n} x_n \ldots x_2 x_1 \tag{4}$$

Eq. (4) is also being represented as Reed-Muller (RM) expansions based on each variable appearance. Variables can be appeared as true form (x_i) or complemented form ($\overline{x_i}$) or mixed form (x_i and $\overline{x_i}$).

B. Fixed Polarity Reed-Muller Expansions

When each variable appears in true or complemented form but not both at the same time as shown in eq.(4) is known as Fixed Polarity Reed-Muller (FPRM) expansion. FPRM expansion provides 2^n different polarities or expansions for a given problem. Example 1 demonstrates the formation of an FPRM expansion.

Example 1: Consider a Boolean expression with the function given by:

$$f_1(x_3,x_2,x_1)=\sum m(3,5,6)=x_1x_2\overline{x_3}+x_1\overline{x_2}x_3+\overline{x_1}x_2x_3 \quad (5)$$

FPRM expansion polarities are defined with binary numbers as

$$< p_j >=< p_n, p_{n-1},\ldots p_1 >$$

$$p_j=\begin{cases}0 & if \quad x_k \quad appears \quad in \quad complemented \quad form\\ 1 & if \quad x_k \quad appears \quad in \quad true \quad form\end{cases} \quad (6)$$

If polarity $(101)_2$ is assigned to a function $f_1(x_3, x_2, x_1)$, then the variables x_1 and x_3 are expressed in true form, and variable x_2 is in complemented form by utilizing $x_i=(1\oplus\overline{x_i})$ and $\overline{x_i}=(1\oplus x_i)$ respectively.

For the given polarity the FPRM expansion for function f_1 is given by:

$$\begin{aligned}&f_1(x_3,x_2,x_1)=x_1x_2\overline{x_3}+x_1\overline{x_2}x_3+\overline{x_1}x_2x_3\\&=\left[x_1(\overline{x_2}\oplus 1)(x_3\oplus 1)\right]\oplus\left[x_1\overline{x_2}x_3\right]+\left[(x_1\oplus 1)(\overline{x_2}\oplus 1)x_3\right]\\&=x_1\oplus x_3\oplus x_1\overline{x_2}\oplus\overline{x_2}x_3\oplus x_1\overline{x_2}x_3\end{aligned} \quad (7)$$

C. Mixed Polarity Reed-Muller Expansions

If each variable in eq. (4) is represented by true or complemented form at the same time, then this form of representation is known as Mixed Polarity Reed-Muller (MPRM) Expansion. 3^n different polarities or expansions are possible in MPRM expansion. The 3^n polarities of MPRM expansion include 2^n polarities of FPRM expansion. Hence, probability of getting a better solution in MPRM is more than that of FPRM. Example 2 illustrates the formation of MPRM expansion.

Example 2: Example considered for FPRM expansion (in example 1) is taken to illustrate the MPRM expansion.

$$f_1(x_3,x_2,x_1)=\sum m(3,5,6)=x_1x_2\overline{x_3}+x_1\overline{x_2}x_3+\overline{x_1}x_2x_3 \quad (8)$$

Ternary variable is used to represent the polarities of MPRM expansion.

$$< p_j >=< p_n, p_{n-1},\ldots p_1 >$$

$$p_j=\begin{cases}0 & if \quad x_k \quad appears \quad in \quad complemented \quad form\\ 1 & if \quad x_k \quad appears \quad in \quad true \quad form\\ 2 & if \quad x_k \quad appears \quad in \quad mixed \quad form\end{cases} \quad (9)$$

If function $f_1(x_3, x_2, x_1)$ is encoded as $(201)_3$, where x_1 is expressed in true polarity, x_2 is in complementary form, and x_3 is represented in mixed form, the MPRM expansion for function f_1 by given polarity is expressed as:

$$\begin{aligned}&f_1(x_3,x_2,x_1)=x_1x_2\overline{x_3}\oplus x_1\overline{x_2}x_3\oplus\overline{x_1}x_2x_3\\&=[x_1(\overline{x_2}\oplus 1)\overline{x_3}]\oplus[x_1\overline{x_2}x_3]\oplus[(x_1\oplus 1)(\overline{x_2}\oplus 1)x_3]\\&=x_1\overline{x_2}\overline{x_3}\oplus x_1\overline{x_3}\oplus x_1\overline{x_2}x_3\oplus x_1\overline{x_2}x_3\oplus x_1x_3\oplus\overline{x_2}x_3\oplus x_3\\&=x_1\overline{x_2}\overline{x_3}\oplus x_1(x_3\oplus 1)\oplus x_1x_3\oplus\overline{x_2}x_3\oplus x_3\\&=x_1\overline{x_2}\overline{x_3}\oplus x_1\oplus\overline{x_2}x_3\oplus x_3\end{aligned} \quad (10)$$

It is inferred from eq. (7) and (10) that judicious choice of input variable polarity in MPRM expansion can provide a better solution than the FPRM expansion. Nine (9) literals are required to represent the function given in example 1 using FPRM. Whereas, only seven (7) literals are sufficient to represent the same function using MPRM expansion. It is expected that the number of switching activity is also get reduced with the literal minimization. The next section describes the tabular technique implementation for MPRM thermal-aware problem realization.

III. Proposed Thermal Aware Mixed Polarity Reed-Muller Approach Using Tabular Technique

A. Area Computation

The thoughtful conversion of Boolean function into MPRM for maximum sharing of product terms considering the optimization parameters by efficient input variable encoding is carried out in this work. A multi-input multi-output Boolean function in the form of pla file is considered as input for the proposed synthesis process. The following steps illustrate the tabular technique implementation for MPRM thermal-aware problem realization. A brief description for polarity conversion procedure is given below.

All the terms present in the Boolean function are listed in Binary form. Don't care conditions are realized in true as well as complementary form to generate canonical representation. Input variables are encoded in mixed polarity, as shown by eq. 9. Then, the input functions are decomposed based on encoding.

Inter polarity conversion takes place according to the chromosome encoding. There can be any of the following three cases –

- 2 to 2 conversion: When a variable is initially in mixed form, '2' and after conversion also the polarity of that variable is '2', then the variable is in mixed form. For such case, the bits of the corresponding variable remain unchanged.
- 2 to 1 conversion: When the variable is initially in mixed form, '2' and the final polarity of the variable is '1', i.e., the variable exists in true form in the final expression, for that all the '0's of the variable are to be replaced by '1' and thus a new term with don't care is generated in the table.
- 2 to 0 conversion: When the variable is in mixed form, '2' initially, and the final polarity of the variable is '0', i.e., the variable exists in complementary form, for that all the '1's of the variable are to be replaced by '0', and thus a new term with don't care is generated in the table.

After generating all the possible new terms for a single variable, they are to be compared with the existing terms to cancel out the similar terms and the table is updated. If two input cubes having same output, but the input is varied by only one literal then that literal is replaced by don't care symbol (–). In this way, steps are repeated for all the input variables in the function to get the reduced MPRM expression.

```
.i  4
.o  2
.p  8
x   y   z   w   f1  f2
1   0   0   0   0   1
1   0   0   1   0   1
0   0   1   0   1   0
0   0   1   1   1   0
0   1   0   0   1   0
1   1   1   0   1   1
1   1   0   1   1   1
0   1   1   1   1   0
.e
```

(a)

x	y	z	w
2	2	1	0

(b)

Fig. 1. (a) '.pla' file representation of Boolean function ('i', 'o' and 'p' represent number of inputs, number of outputs and product terms respectively); (b) Input variable encoding ('x' and 'y' are in mixed form; 'w' is in complementary form and 'z' is in true form).

An arbitrary Boolean function is considered as an example case and it is shown in Fig. 1(a). The chromosome encoding for the example case is shown in Fig. 1(b). The translation of input Boolean function and area computation using tabular technique is shown below.

The two output functions are:

$$f_1 = \bar{x}\bar{y}z\bar{w} + \bar{x}\bar{y}zw + \bar{x}y\bar{z}\bar{w} + xyz\bar{w} + xy\bar{z}w + \bar{x}yzw \quad (11)$$

$$f_2 = x\bar{y}\bar{z}\bar{w} + x\bar{y}\bar{z}w + xyz\bar{w} + xy\bar{z}w \quad (12)$$

Generally, Boolean functions are expressed in terms of AND- OR function. As f_1 and f_2 are represented in disjoint cube form, so it can be represented as:

$$f_1 = \bar{x}\bar{y}z\bar{w} \oplus \bar{x}\bar{y}zw \oplus \bar{x}y\bar{z}\bar{w} \oplus xyz\bar{w} \oplus xy\bar{z}w \oplus \bar{x}yzw \quad (13)$$

and, $$f_2 = x\bar{y}\bar{z}\bar{w} \oplus x\bar{y}\bar{z}w \oplus xyz\bar{w} \oplus xy\bar{z}w \quad (14)$$

Table I shows the input polarity conversion based on encoding, as shown in Fig. 1(b). Variable *x* and *y* are represented in mixed polarity form so, no new term is generated. But new term will be generated for z and w, where the variables are expressed in true and complementary form respectively. The redundant terms noted with *a, b, c, d* and *e* get eliminated, and the terms noted with *f* forms a new term by replacing one literal with don't care.

After polarity conversion, the final MPRM output for function f_1 and f_2 are represented as:

$$f_1 = \bar{x}y\bar{w} \oplus xyz \oplus xy\bar{w} \oplus xy \oplus \bar{x}z \quad (15)$$

$$f_2 = x\bar{y}z \oplus x\bar{y} \oplus xyz \oplus xy\bar{w} \oplus xy \oplus \bar{x}z \quad (16)$$

Shared terms are: $xyz, xy\bar{w}, xy$

It is observed that primary function requires 8 product terms with 32 literals whereas, final function requires 7 product terms with 18 literals (where 3 product terms are shared among function f_1 and f_2).

B. Power Estimation Using Switching Activity

In CMOS circuits, the dynamic dissipation is the main contributor to power consumption, which is caused by charging and discharging the load capacitances. It can be modeled as:

$$P_{dyn} \approx P_{swt} = \alpha_L C_L V_{DD}^2 f + \sum_i \alpha_i C_i V_{DD}(V_{DD} - V_T) f \quad (17)$$

Where, P_{dyn} and P_{swt} represent the dynamic and switching power respectively. α_L and α_i are the switching activity at the load and internal node respectively. The capacitance at the load and internal gates are represented by C_L and C_i respectively. Supply voltage, threshold voltage, and frequency of operation are given by V_{DD}, V_T, and f respectively.

Eq. (17) illustrates that, except for those of switching activity, all other parameters are user/manufacturer defined at a particular technology. Switching activity is the only parameter that needs to be estimated for technology-independent power optimization. Expected number of signal transitions at the outputs of the gates of a combinational logic circuit is defined as switching activity. This work follows the same procedure used in the reference [32] to estimate switching activity. Let us consider that initial inputs are uncorrelated and statically independent of each other, represented as:

$$\text{Prob}(\text{input} = 1) = \text{Prob}(\text{input} = 0) = 0.5 \quad (18)$$

The probability of the output of a gate when its inputs are changed from the previous state is estimated by:

$$\text{Prob}(\text{present} = 0) \cdot \text{Prob}(\text{past} = 1) + \text{Prob}(\text{present} = 1) \cdot \text{Prob}(\text{past} = 0) \quad (19)$$

The switching probability follows the stationary random process, and probabilistic description does not change over a given period. Then, switching activity of logic gate (α_g) is given by:

$$\alpha_g = 2 \cdot \text{Prob}_{op=0} \cdot \text{Prob}_{op=1} \quad (20)$$

TABLE I. Input Variable Polarity Transformation Using Tabular Technique

Input		Term generated by z		Term generated by w		Terms get canceled/ modified			Remaining terms	
x y z w	$f_1 f_2$	x y z w	$f_1 f_2$	x y z w	$f_1 f_2$	x y	z w	$f_1 f_2$	x y z w	$f_1 f_2$
1 0 0 0	0 1	1 0 1 0	0 1	1 0 1 0	0 1	~~1 0~~	~~0 1~~	*a*		
		1 0 – 0	0 1	1 0 – 0	0 1	~~1 0~~	~~0 1~~	*b*		
1 0 0 1	0 1	1 0 1 1	01	1 0 1 0	0 1	~~1 0~~	~~0 1~~	*a*	1 0 1 –	0 1
				1 0 1 –	0 1					
		10 – 1	01	1 0 – 0	0 1	~~1 0~~	~~0 1~~	*b*	1 0 – –	0 1
				1 0 – –	0 1					
0 0 1 0	1 0	0 0 1 0	1 0	0 0 1 0	1 0	~~0 0~~	~~1 0~~	*c*		
0 0 1 1	1 0	0 0 1 1	1 0	0 0 1 0	1 0	~~0 0~~	~~1 0~~	*c*		
				0 0 1 –	1 0	0 0	1 0	*f*		
0 1 0 0	1 0	0 1 1 0	1 0	0 1 1 0	1 0	~~0 1~~	~~1 0~~	*d*	0 1 – 0	1 0
		0 1 – 0	1 0	0 1 – 0	1 0					
1 1 1 0	1 1	1 1 1 0	1 1	1 1 1 0	1 1	~~1 1~~	~~1 1~~	*e*		
1 1 0 1	1 1	1 1 1 1	1 1	1 1 1 0	1 1	~~1 1~~	~~1 1~~	*e*	1 1 1 –	1 1
				1 1 1 –	1 1					
		1 1 – 1	1 1	1 1 – 0	1 1				1 1 – 0	1 1
				1 1 – –	1 1				1 1 – –	1 1
0 1 1 1	1 0	0 1 1 1	1 0	0 1 1 –	1 0	0 1	1 0	*f*	0 – 1 –	1 0
				0 1 1 0	1 0	~~0 1~~	~~1 0~~	*d*		

The generalized expression for switching activity for an '*i*' input AND gate (α_{AND}) with input switching probability '0.5' is given by:

$$\alpha_{AND} = 2 \cdot (0.5)^{i} \cdot [1-(0.5)^{i}] \quad (21)$$

Second level ON-probability of XOR gates may be computed by '$P \cdot 0.5^{i}$'. Where 'i' is the inputs realization of a function with '*P*' ON-terms. The probable switching activity of the node is given by:

$$\alpha_{XOR} = 2 \cdot \left[P \cdot 0.5^{i}\right] \cdot \left[1-(P \cdot 0.5^{i})\right] \quad (22)$$

The power consumption of a MPRM circuit is the sum of power of AND gates and XOR gates. Assuming that 'n' is the set of nodes in MPRM circuits, then the total switching activity is given by:

$$\alpha_{total} = \sum_{n} \alpha_{AND} + \sum_{n} \alpha_{XOR} \quad (23)$$

C. Power Density

The amount of power drawn per unit area defines the power density of a circuit. It can be calculated by taking the ratio of total switching activity and area of the circuit.

$$Pd_{MPRM} = \alpha_{total} / A_{MPRM} \quad (24)$$

Where, Pd_{MPRM}, α_{total} and A_{MPRM} represent the power density, overall switching activity and total area of an MPRM realized network. The power density is estimated for a particular offspring chromosome to determine the thermal effect. Lower the power density better is the distribution of temperature among the different modules within a chip. This has also been verified by finding the absolute temperature (in °C) using Cadence and HotSpot tool.

IV. Non-Dominated Sorting Based Genetic Algorithm-II For Proposed Thermal-aware Realization

Classical search techniques like genetic algorithm (GA) disperse the optimum solution throughout the search space and can find one optimal solution for a given weight combination in a single run when multiple objectives are there. All possible weight combinations are mandatory to go through to obtain the optimum solution. For which the execution time consumes much delay to find the optimum solution. An elitist non-dominated sorting based multi-criteria decision-making algorithm called non-dominated genetic algorithm-II (NSGA-II) is employed to overcome the above inconsistency. NSGA-II is a fast and improved multi-objective evolutionary algorithm (MOEA) with computational complexity $O(XY^2)$, where 'X' is the number of objective parameters, and 'Y' is the population size. Fitness estimation or sharing parameters are replaced with the rank assignment and front selection using non-dominated sorting and crowding distance calculation in NSGA-II for better elitism and fast convergence toward an optimum solution. The detailed procedure of NSGA-II is discussed in [33]. Configurable parameters, optimization objectives and constraints used for proposed algorithm are discussed elaborately in this section.

A. Chromosome Structure

Efficient chromosome structure can be encoded for an 'm' input combinational logic circuit by ternary bit string of length 'm'. The'm' input variables (l_1, l_2, l_3, ..., l_m) represents complementary, true and mixed polarity based on ternary operator bits {0, 1, 2}. If the p^{th} bit is '1', it denotes that the p^{th} input variable is implemented in true polarity whereas, if the q^{th} and r^{th} bits are '0'and '2' respectively, it symbolizes that the q^{th} and r^{th} inputs are realized in complementary and mixed polarity respectively.

B. Front Selection and Rank Assignment Based on Non-domination

Chromosomes in each front are assigned fitness based on their rank values or the front in which they exist. Chromosomes in the first front are designated with the highest rank value as 'one'(1) and individuals in the second are assigned the rank value as two (2) and so on.

1. **Crowding Distance Calculation**:Crowding distance (i_{dist}) is another fitness parameter which depicts the density of a solution in a population. i_{dist} can be calculated for each objective function by evaluating the Euclidean distance between individual chromosomes in a front by considering '*n*' objective functions in the '*n*' dimensional hyperspace.
2. **Parent selection**:A chromosome is selected as a parent if its rank is lesser than the other. If the ranks of chromosomes are same then the individual having higher crowding distance is selected. The selected parent chromosomes generate next-generation chromosomes using crossover and mutation operators.

C. Genetic Operators

Crossover and mutation are the two inherent mechanisms of the NSGA-II algorithm. They introduce the variation within the generated offspring and converge the output solution towards the optimal solution. It is observed from the literature that better offspring is generated by considering 90% crossover and 10% mutation in NSGA-II based multi-objective evolutionary algorithms [8]. For the proposed approach, the same method is followed. However, three other experiments (70% crossover and 30% mutation, 80% crossover and 20% mutation, 100% crossover) were carried out by varying crossover and mutation percentage but it has been observed that more diversity in population is there if 90% crossover and 10% mutation is considered and good result is obtained.

1. **Crossover**: During crossover operation, two-parent chromosomes '*x*' and 'y' from the initial population mates to produce two new offspring 'co_1' and 'co_2' at randomly selected crossover points. Two-point crossover methods converge the solution faster towards the optimum solution than that of single-point crossover. Parent chromosomes selection is biased towards the chromosomes with better fitness value ('elite group'). Chromosomes with rank one (1) are considered as elite group. The selection of parent chromosomes from elite groups or from entire population to participate in crossover operation depends on the generation of a uniform random number between '0' and '1'. If the number is greater than or equal to '0.5' then the parents for crossover is chosen from the elite group; otherwise, parents are selected from the entire population. The threshold for elite group is considered as '0.5' for selecting best-fit chromosome to participate in the crossover operation to generate better offspring. Let, the size of population is 'p' and the cardinality of elite group is 'q'. Then the probability of selecting a chromosome from elite group is 0.5/q + 0.5/p.Whereas, probability of chromosome selecting from entire population is 0.5/p. The probability of selecting chromosome from elite group is more than that of entire population, because 'q' is much smaller than 'p'. This method selects best-fit chromosomes to participate in the crossover operation and generates better offspring as compared to truly random one [34]. Two crossover positions (cp_1 and cp_2) are randomly selected within the chromosome string length, and the alleles are exchanged between the two selected individuals as shown in Fig. 2(a) and 2(b). Fig. 2 (a) and (b) show the different outcomes of the same parent chromosomes using crossover operation method 1 and method 2 respectively. A check is made after each generation with the already generated chromosomes, and duplicate chromosomes are eliminated.

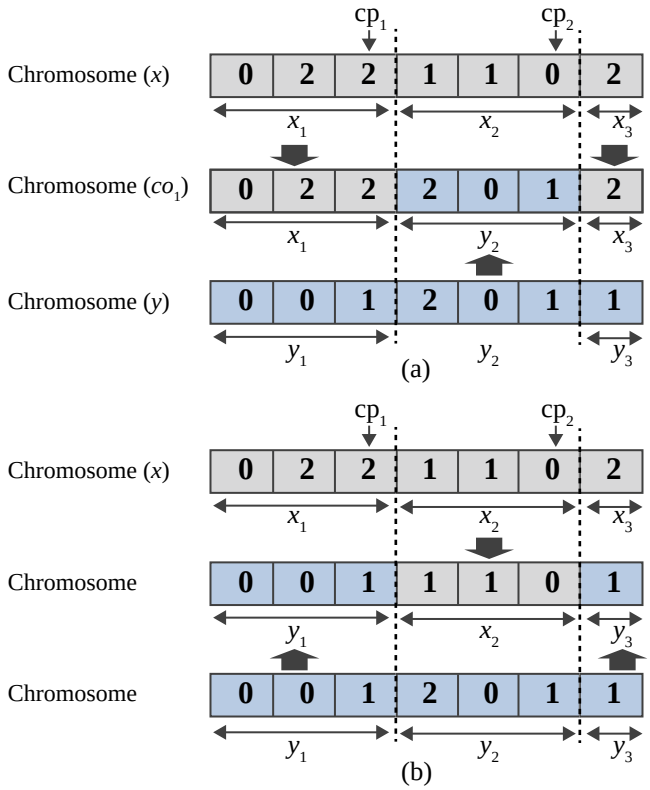

Fig. 2. (a) Crossover operation method 1; (b) Crossover operation method 2.

2. **Mutation**: Mutation enables the genetic diversity from generation to generation. Mutation prohibits falling off all solutions in the population into a local optimum. 10% of the 'N' offspring population is contributed by mutant chromosomes using mutation. Mutation operation is performed by selecting few random bit positions called mutation points (mp) and the polarity of that selected position is altered by the roulette wheel selection methodology as shown in Fig. 3(a). To increase the randomness, the mutation points are chosen randomly within a range of 1 to 'n' (where 'n' is the length of the chromosome). For an example case, a chromosome (m) is participating in mutation operation from the present generation; randomly three positions are selected as a mutation point (mp_1, mp_2, and mp_3). Inter-conversion of polarity that is, the positive, negative and mixed polarity is done using roulette wheel criterion and remaining bits get unaltered. The newly generated offspring becomes the chromosome of the next generation.

   Fig. 3(b) illustrates the operation of the roulette wheel criterion. A random number (R_n) between '0' and '1' is generated for each mutation point, and if the generated random number (R_n) is greater than or equal to '0.5', the wheel position moves clockwise otherwise anti-clockwise. Depending on the elevated position, the polarity of the mutation point will change. Choosing a random number based on some prior information (like range, mean, variance, etc.) is a convex optimization problem (which is determined by entropy of objective function). With finite range, maximum entropy is given by uniform probability distribution function. Other distributions will have less entropy than the uniform probability distribution in the same range.

The proposed NSGA-II algorithm contributes 'N' chromosomes using the selected parents by crossover and mutation methods. Generated 'N' offspring and 'N' parents contribute as '2N' numbers of next-generation population.

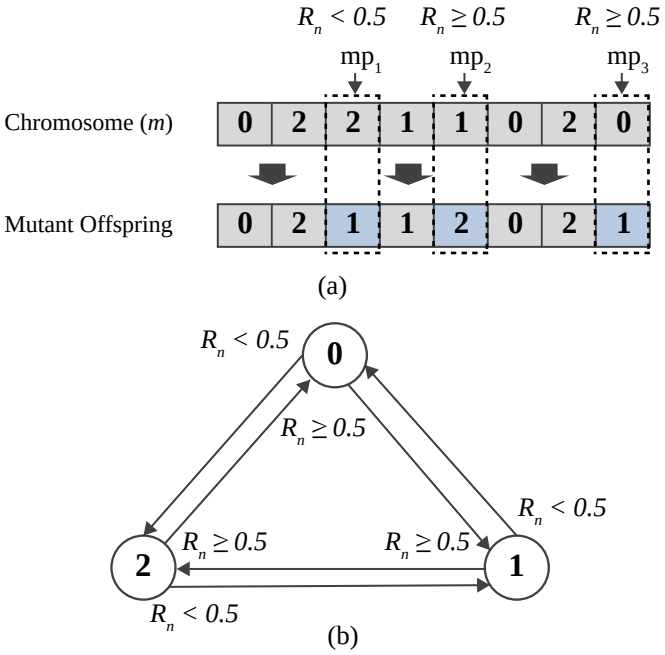

Fig. 3 (a) Mutation operation; (b) Roulette wheel criteria for bit manipulation in mutation operation.

V. Results and Related Discussions

Proposed thermal-aware mixed polarity AND-XOR realization of logic circuits have been implemented using NSGA-II in LINUX based C++ platform on a Pentium IV machine with 3-GHz clock frequency and 4-GB RAM memory. The algorithm is applied to MCNC and LGSynth93 benchmark suite [35] for experimentation. In the proposed work, NSGA-II based optimization approach is proposed for simultaneous reduction of area, power, and temperature. We have targeted logic level for optimization to reduce the cooling cost through heat-sink. At logic level, absolute values of area, power, and temperature are unknown. Therefore, for area reduction, reduction of product term is considered. To optimized power, switching activity is reduced. And for temperature reduction, power density is reduced in the cost metric. NSGA-II provides the Pareto optimal solution set consisting of area best, power best, power density best and optimum solution considering all the three parameters. To obtain the actual silicon area (in μm^2), power dissipation (in nW) and absolute temperature (in °C) Cadence (Genus and Innovus) and HotSpot tools are used. Cadence and HotSpot Electronics Design Automation (EDA) software packages are involved for simulating the digital and analog circuits. We have generated the graphical design specification information interchange (GDS-II) report after layout design for best and optimum solutions obtained using the proposed algorithm for each benchmark circuit, but there is no hardware implementation (chip fabrication) of the circuit. The total discussion of result is divided into two sections. The first section of result concerns the area, power and power density based result using NSGA-II approach. The next section briefly describes the implementation of physical design at 45 nm technology using Cadence Genus and Innovus Implementation tool. Then absolute temperature estimation using HotSpot tool is presented.

A. Result Based on NSGA-II

The '.pla' based circuits of MCNC and LGSynth93 benchmark suit are considered as an input circuits which are to be optimized in terms of area, power and temperature optimization. The circuits are decomposed into MPRM expansion based on input variable polarity

encoding as explained in chromosome structure. NSGA-II is used to find efficient chromosome polarity based on area, power, and power density. Twenty (20) benchmark circuits are tested for experimentation. Table II gives the parameters and evolution operator's settings for the proposed NSGA-II based approach.

TABLE II. Parameters and Evolution Operator's Settings for the Proposed NSGA-II Approach

Parameter	Value
No. of initial population	100.00
Total no. of iteration	200.00
Crossover probability	0.9
Mutation probability	0.1
Crossover operation	Two-point crossover method
Mutation operation	Bit mutation based on Roulette wheel criteria
Termination criterion	Max. no. of iteration

To verify the efficiency of the proposed approach using NSGA-II, the proposed best and optimized results of MPRM circuits are compared with previously published best and optimum results of FPRM [36], Shared Reed-Muller Decision Diagram (SRMDD) [22], MPRM [10], AND-Inverter Graphs (AIGs) [37] and GA based FPRM [38] decomposed circuits. A set of solutions (called Pareto optimal solutions) are obtained comprising of the individual best solutions ('Area Best', 'Power Best' and 'Power density Best') and 'optimum solution'. An area comparative study of the proposed approach with FPRM, SRMDD, MPRM, AIGs, and GA based FPRM is presented in Table III. For power comparison, the proposed method is compared with FPRM, AIGs and GA based FPRM solutions, which are reported in Table IV. For power density based comparison, the proposed power density solutions are compared with SRMDD and AIGs based solutions and reported in Table V. In Tables III, IV and V, the first column shows the circuit name with which experimentation is carried out. The second and third columns of Tables III, IV and V represent the proposed best and optimum solution for area, power and power density, respectively. The "Save Best" and "Save Opt" columns in Tables III, IV and V shows the percentage savings of the proposed approach with respect to the existing works reported in the literature. The average percentage saving is calculated and reported in the last row of Tables III, IV and V. The percentage savings referred to in the column "Save Best" and "Save Opt" of Tables III, IV and V are calculated by the following Eq. (25) and (26).

$$\text{Save Best} = \left(\frac{\text{Existing}_{\text{solution}} - \text{Best solution}}{\text{Existing}_{\text{solution}}} \text{X100} \right)\% \quad (25)$$

$$\text{Save Opt} = \left(\frac{\text{Existing}_{\text{solution}} \quad \text{Optimum solution}}{\text{Existing}_{\text{solution}}} \text{X100} \right)\% \quad (26)$$

The percentage savings for the proposed best solution and proposed optimum solution are represented by "Save Best" and "Save Opt" as referred in Eq. (25) and (26), respectively. The "Best solution", "Optimum solution" and "$\text{Existing}_{solution}$" represent the proposed NSGA-II based best solution, NSGA-II based optimum solution and existing reported works of literature, respectively.

From Table III, it is observed that the chromosome with the proposed area best solution of NSGA-II save 28.61%, 22.85%, 29.45%, 30.45% and 35.19% area compared to that of FPRM, SRMDD, MPRM, AIGs, and GA based FPRM based results respectively. When the proposed optimum solution comparative study is performed with respect to FPRM, SRMDD, MPRM, AIGs, and GA based FPRM results then proposed optimum solution shows an area saving of 18.42%, 10.92%, 15.94%, 6.86% and 23.51% compared to that of FPRM, SRMDD, MPRM, AIGs, and GA based FPRM based results, respectively.

When power-based realization is compared in Table IV, it is observed that FPRM, AIGs, and GA based FPRM solutions consume

TABLE III. Area Comparative Study Of the Proposed MPRM Realization

Circuits	Proposed approach		FPRM [36]			SRMDD [22]			MPRM [10]			AIGs [37]			GA based FPRM [38]		
	Area Best	Optimum solution	Area	Save Best	Save Opt	Area	Save Best	Save Opt	Area	Save Best	Save Opt	Area	Save Best	Save Opt	Area	Save Best	Save Opt
5xp1	49	49	61	19.67	19.67	61	19.67	19.67	61	19.67	19.67	66	25.76	25.76	61	19.67	19.67
9sym	87	116	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
alu2	257	314	-	-	-	225	-14.22	-39.56	-	-	-	333	22.82	5.71	225	-14.22	-39.56
alu4	993	1485	-	-	-	-	-		2438	59.27	39.09	719	-38.11	-106.54	3683	73.04	59.68
clip	118	118	-	-	-	206	42.72	42.72	182	35.16	35.16	-	-	-	206	42.72	42.72
cm162a	25	25	25	0.00	0.00	25	0.00	0.00	-	-	-	38	34.21	34.21	25	0.00	0.00
cm163a	18	18	18	0.00	0.00	18	0.00	0.00	-	-	-	-	-	-	18	0.00	0.00
con1	9	10	-	-	-	-	-	-	14	35.71	28.57	-	-	-	-	-	-
cu	21	23	37	43.24	37.84	-	-	-	-	-	-	-	-	-	-	-	-
inc	34	37	106	67.92	65.09	48	29.17	22.92	34	0.00	-8.82	87	60.92	57.47	-	-	-
misex1	16	19	20	20.00	5.00	32	50.00	40.63	13	-23.08	-46.15	-	-	-	-	-	-
misex2	55	57	87	36.78	34.48	-	-	-	-	-	-	84	34.52	32.14	-	-	-
misex3c	296	757	-	-	-	-	-	-	1421	79.17	46.73	533	44.47	-42.03	1831	83.83	58.66
pm1	19	21	27	29.63	22.22	-	-	-	-	-	-	30	36.67	30.00	27	29.63	22.22
rd53	15	24	20	25.00	-20.00	20	25.00	-20.00	20	25.00	-20.00	-	-	-	20	25.00	-20.00
rd73	43	43	-	-	-	64	32.81	32.81	63	31.75	31.75	-	-	-	63	31.75	31.75
rd84	73	73	107	31.78	31.78	-	-	-	107	31.78	31.78	-	-	-	107	31.78	31.78
sao2	74	85	100	26.00	15.00	-	-	-	76	2.63	-11.84	-	-	-	-	-	-
table3	175	219	-	-	-	-	-	-	401	56.36	45.39	-	-	-	1945	91.00	88.74
x2	17	27	30	43.33	10.00	30	43.33	10.00	-	-	-	36	52.78	25.00	30	43.33	10.00
Av. % Savings w.r.t Proposed Solution				**28.61**	**18.42**		**22.85**	**10.92**		**29.45**	**15.94**		**30.45**	**6.86**		**35.19**	**23.51**

28.71%, 85.35% and 50.27% more power with respect to the proposed best power-based solutions respectively. When proposed optimum power-based solutions are compared, then the FPRM, AIGs, and GA based FPRM solutions consume 11.72%, 81.19%, and 41.96% more power than that of the proposed solutions, respectively. The best power density based solutions show 23.68% and 69.83% reduction in power density compared to that of SRMDD and AIGs based solutions in Table V. The optimum power density based solutions provide 10.90% and 70.02% better results than that of SRMDD and AIGs based solutions respectively. Fig. 4 shows the Pareto-optimal graph for "*table3*" benchmark circuit.

The solutions nearer to the origin form the Pareto-optimal front, which are optimal with respect to area, power, and power density. The solutions nearer to each axis represent the best solutions. The last column of Table V reports the total CPU time required (in CPU seconds) to execute the algorithm in an identical platform.

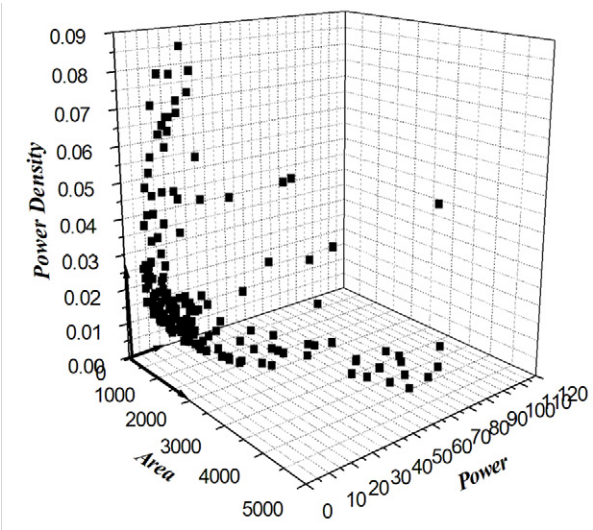

Fig. 4. Pareto optimal graph of '*table3*' benchmark circuit using NSGA-II.

B. Physical Design Implementation At 45Nm Technology

At logic level, evenly distributed or average power density is considered. NSGA-II algorithm is used to determine the optimum input variable polarity based on area, power, and power density. Initially, the dynamic power is estimated by calculating the switching activity, and the area is estimated by calculating the total number of product terms. To calculate the power density for a particular logic, the ratio of power to area is considered. Then the optimized realization is synthesized using Cadence Genus digital design platform. The synthesized netlist is implemented to have physical design at 45nm technology using Cadence Innovus platform. After physical design realization, Innovus generates the floorplan information (.flp file) and power profile (.pptrace file). In floorplan information, the synthesized logic is represented with different modules with their height, width, X and Y coordinates to allocate the position of a particular module within the chip. In the power profile, the power dissipation information of each module is given. The floorplan information and power profile are given as input to the HotSpot tool for generating the temperature profile. Based on floorplan information and power profile given, the HotSpot tool generates the temperature profile for each module in degree centigrades (°C). Fig. 5 shows the schematic flow-diagram of temperature generation using HotSpot tool. For an example case, the floorplan information and power profile of "rd53" benchmark circuit is shown in Fig. 6 and Fig. 7, respectively. The corresponding floorplan generation is shown in Fig. 8. The temperature profile generation using HotSpot tool using the floorplan information and power profile is shown in Fig. 9.

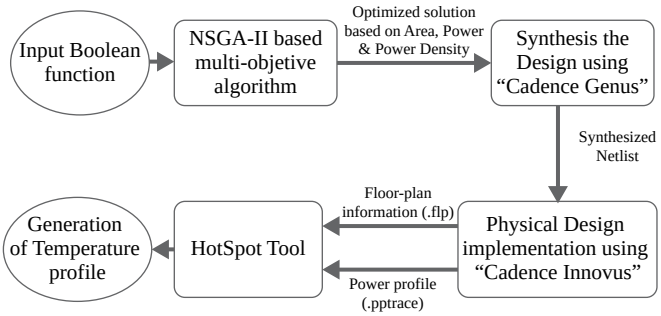

Fig. 5. Schematic Flow-diagram of temperature profile generation using the HotSpot tool.

```
# Floorplan information
# Line Format: <unit-name>    <width>    <height>    <left-x>    <bottom-y>
# all dimensions are in meters

g458    0.0000540    0.0000501    0.0028400    0.0017100
g460    0.0000540    0.0000501    0.0020000    0.0028290
g459    0.0000540    0.0000501    0.0024800    0.0028290
g461    0.0000560    0.0000501    0.0028400    0.0024870
g462    0.0000540    0.0000501    0.0025600    0.0024870
g463    0.0000410    0.0000501    0.004800     0.0028290
g464    0.0000540    0.0000501    0.0025600    0.0017100
g467    0.0000440    0.0000501    0.0040000    0.0017100
g466    0.0000440    0.0000501    0.0068000    0.0028290
g469    0.0000620    0.0000501    0.0027600    0.0028290
g465    0.0000460    0.0000501    0.0022000    0.0028290
g468    0.0000440    0.0000501    0.0076000    0.0028290
g470    0.0000540    0.0000501    0.0012000    0.0017100
g473    0.0000480    0.0000501    0.0023200    0.0028290
g471    0.0000480    0.0000501    0.0016000    0.0024870
g472    0.0000460    0.0000501    0.0032000    0.0024870
g474    0.0000440    0.0000501    0.0044000    0.0024870
```

Fig. 6. Floorplan information of the "*rd53*" benchmark circuit generated by Cadence Innovus tool.

```
# Power profile
# Line Format:   dissipation>
# All power information's are in Watts

g458    g460    g459    g461    g462    g463    g464    g467    g466    g469    g465
        g468    g470    g473    g471            g472    g474

0.449000        0.448000        0.873000        0.268000        0.558000        0.100000
                0.592000        0.078000        0.157000        0.664000        0.040000
                0.078000        0.441000        0.203000        0.187000        0.149000
                0.079000
```

Fig. 7. Power profile of the "*rd53*" benchmark circuit generated by Cadence Innovus tool.

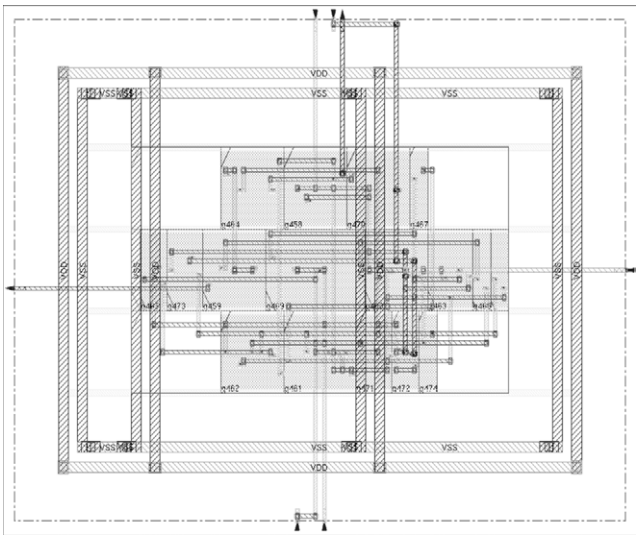

Fig. 8. Floorplan of the "*rd53*" benchmark circuit generated by the Cadence Innovus tool.

TABLE IV. Power Comparison Of the Proposed MPRM Realization

Circuits	Proposed approach		FPRM [36]			AIGs [37]			GA based FPRM [38]		
	Power Best	Optimum solution	Power	Save Best	Save Opt	Power	Save Best	Save Opt	Power	Save Best	Save Opt
5xp1	5.274	5.274	12.29	57.09	57.09	30.979	82.98	82.98	12.29	57.09	57.09
9sym	3.003	3.003	-	-	-	-	-	-	-	-	-
alu2	12.747	12.747	-	-	-	112.370	88.66	88.66	22.24	42.68	42.68
alu4	20.752	70.842	-	-	-	240.279	91.36	70.52	108.40	80.86	34.65
clip	4.568	4.568	-	-	-	-	-	-	18.85	75.77	75.77
cm162a	4.523	4.523	5.48	17.46	17.46	20.770	78.22	78.22	5.48	17.46	17.46
cm163a	3.599	5.094	5.09	29.29	-0.08	-	-	-	5.09	29.29	-0.08
con1	2.097	2.330	-	-	-	-	-	-	-	-	-
cu	7.175	7.197	4.99	-43.79	-44.23	-	-	-	-	-	-
inc	6.556	6.556	13.23	50.45	50.45	35.389	81.47	81.47	-	-	-
misex1	4.929	4.929	6.46	23.70	23.70	-	-	-	-	-	-
misex2	5.228	8.654	9.53	45.14	9.19	84	93.78	89.70	-	-	-
misex3c	5.037	8.910	-	-	-	162.090	96.89	94.50	67.42	92.53	86.78
pm1	4.288	5.899	6.56	34.63	10.08	15.900	73.03	62.90	6.28	31.72	6.07
rd53	4.580	4.580	5.61	18.36	18.36	-	-	-	5.61	18.36	18.36
rd73	7.764	7.764	-	-	-	-	-	-	13.48	42.40	42.40
rd84	12.459	12.459	20.18	38.26	38.26	-	-	-	20.18	38.26	38.26
sao2	1.825	4.654	2.49	26.71	-86.91	-	-	-	-	-	-
table3	5.425	5.703	-	-	-	-	-	-	26.75	79.72	78.68
x2	3.112	3.112	5.9	47.25	47.25	17.090	81.79	81.79	5.91	47.34	47.34
Av. % Savings of Proposed Approach				**28.71**	**11.72**		**85.35**	**81.19**		**50.27**	**41.96**

TABLE V. Power Density Comparison Of the Proposed MPRM Realization

Circuits	Proposed approach		SRMDD [22]			AIGs [37]			CPU time (s)
	Power density Best	Optimum solution	Pow_Den	Save Best	Save Opt	Pow_Den	Save Best	Save Opt	
5xp1	0.107	0.107	0.191	43.98	43.98	0.396	72.98	72.98	118.40
9sym	0.025	0.025	-	-	-	-	-	-	140.65
alu2	0.037	0.040	0.084	55.95	52.38	0.324	88.58	87.65	126.48
alu4	0.008	0.047	-	-	-	0.279	97.13	83.15	481.84
clip	0.038	0.038	0.092	58.70	58.70	-	-	-	78.82
cm162a	0.180	0.180	0.087	-106.90	-106.90	0.536	66.42	66.42	155.39
cm163a	0.199	0.283	0.283	29.68	0.00	-	-	-	148.26
con1	0.231	0.233	-	-	-	-	-	-	106.15
cu	0.247	0.312	-	-	-	-	-	-	117.16
inc	0.139	0.177	0.181	23.20	2.21	0.373	62.73	52.55	111.26
misex1	0.154	0.259	0.254	39.37	-1.97	-	-	-	147.24
misex2	0.149	0.151	-	-	-	0.333	55.26	54.65	29.92
misex3c	0.150	0.011	-	-	-	0.257	41.63	95.72	97.13
pm1	0.154	0.280	-	-	-	0.494	68.83	43.32	170.89
rd53	0.188	0.190	0.256	26.56	25.78	-	-	-	105.87
rd73	0.121	0.180	0.211	42.65	14.69	-	-	-	216.26
rd84	0.097	0.171	-	-	-	-	-	-	104.41
sao2	0.054	0.054	-	-	-	-	-	-	123.21
table3	0.016	0.026	-	-	-	-	-	-	805.14
x2	0.110	0.115	0.144	23.61	20.14	0.438	74.89	73.74	131.44
Av. % Savings of Proposed Approach				**23.68**	**10.90**		**69.83**	**70.02**	

Note: (–) indicates that the results are not reported or unavailable.

```
# Temperature profile
# Line Format:  <unit-name>      <temperature>
# All temperatures are in °C

g458   g460   g459   g461   g462   g463   g464   g467   g466   g469   g465
       g468   g470   g473   g471          g472   g474

66.25  66.24  72.15  63.60  67.77  61.83  68.24  61.33  62.68  68.05  60.65
       61.33  66.14  63.18  62.93         62.43  61.35

Maximum Temperature = 72.15 °C
Minimum Temperature = 60.65 °C
```

Fig. 9. Temperature profile of the "*rd53*" benchmark circuit generated by the HotSpot tool.

Cadence (Genus and Innovus) and HotSpot tools are electronic design automation tools used for simulating the digital and analog circuits. We have generated the GDS-II report for best and optimum solutions for each benchmark circuit. Netlist, Synopsis Design Constraints (SDC) library and Library Exchange Format (LEF) files at 45nm technology are provided as input to the Cadence tool. The above process generates floor-plan information (.flp) and power profile (.pptrace), which act as input to the HotSpot tool for calculating absolute temperature profile. Thermal packaging used in HotSpot tool to generate temperature profile are ambient temperature (45.5 °C), chip thickness (0.15mm), convection capacitance (140.4 J/K), convection resistance (5 K/W), heat sink side (60mm), heat sink thickness (6.9mm), spreader side (30mm), spreader thickness (1mm), chip to spreader interface thickness (0.020mm). The dynamic thermal management (DTM) approach is applied to the proposed method by the HotSpot tool. The HotSpot tool has an in-built thermal management technique, where the threshold thermal value can be set to restructure the model to trim down the peak temperature. By default, it is 82°C, so we kept the threshold value as same for our realization. If for a particular placement of logic cells, depending on its power value and location of each cell, temperature increases beyond 82°C, then thermal model of HotSpot tool dynamically changes the relative placement of the cells such that temperature becomes below 82°C. This technique is called "dynamic thermal management" of HotSpot tool. NSGA-II provides the Pareto optimal solution set consisting of best and optimum solution based on area, power and power density. Only the solutions with the best area, best power, best power density and optimum solution consisting of area, power and power density (4 solutions) are processed further for physical design implementation using the Cadence tool. NSGA-II optimized circuits are driven into the physical design synthesis level and area (μm²), power (nW) and temperature (°C) values are reported in Table VI.

Second, third and fourth columns with 'Best_area', 'Best_ power' and 'Best_peak_Temp' report the standard cell area, power consumption and peak temperature generated by best area, best power and best power density solution of NSGA-II respectively. The next three columns report the same for the optimal solution. Comparative analysis with SRMDD and espresso decomposed AND-INVERTER GRAPH (AIG) structure [22], [37] is reported in Table VI. The last column of Table III, indicates the maximum CPU time (in seconds) to implement a benchmark circuit among all the cases (best solutions and optimal solution) in an identical platform. The average percentage savings referred in the last three rows of Table VI is calculated by the following equation.

$$\text{Savings}_{\text{Average}} = \left(\frac{\text{Earlier}_{\text{solution}} - \text{Proposed}_{\text{solution}}}{\text{Earlier}_{\text{solution}}} \text{X100} \right)\% \quad (27)$$

Average percentage savings is represented by "$\text{Savings}_{Average}$" as referred in Eq. (27). "$\text{Proposed}_{solution}$" and "$\text{Earlier}_{solution}$" represent the proposed approach based solution and earlier literature reported solutions, respectively.

Fig. 10, 11, and 12 show the average percentage improvement of the proposed results reported in Table VI. Fig. 10, 11 and 12 depict that the best solution and optimum solution save 75.21% (76.20%) and 73.69% (74.82%) standard cell area than that of SRMDD-based best solution (SRMDD-based optimum solution), respectively. The best peak temperature and optimum peak temperature are reduced by 13.52% (17.06%) and 12.49%(16.08%) than that of SRMDD-based best solution (SRMDD-based optimum solution) respectively. Best area, best power and best peak temperature based solutions of MPRM expansion save 8.80%, 29.09% and 3.89% area, power, and peak temperature respectively when compared with espresso decomposed AIGs structure-based solutions. When optimal solution from Pareto-Optimal solution set is compared, it shows the average savings of 26.20% power and 2.70% peak temperature than that of espresso decomposed AIGs structure solutions at the cost of 4.39% increase in area.

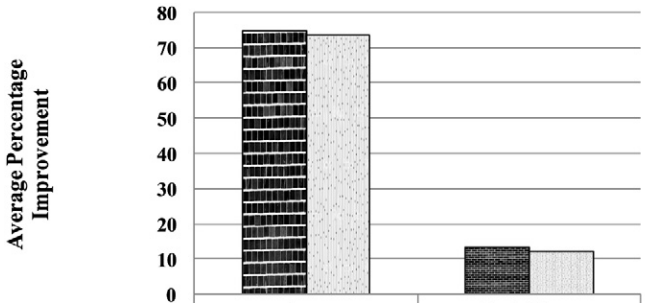

Fig. 10. Average percentage savings of the proposed approach w.r.t. SRMDD best solutions [22].

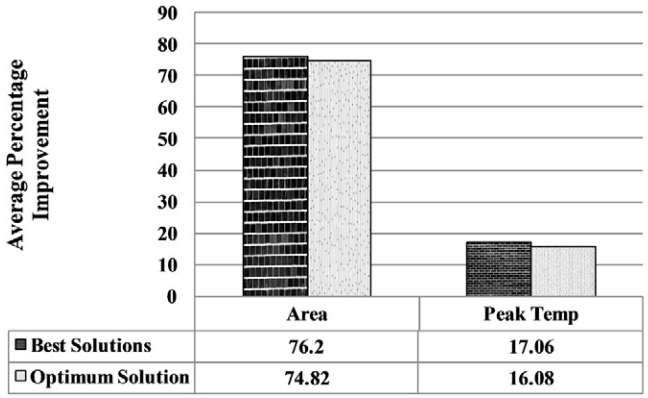

Fig. 11. Average percentage savings of the proposed approach w.r.t. SRMDD optimum solutions [22].

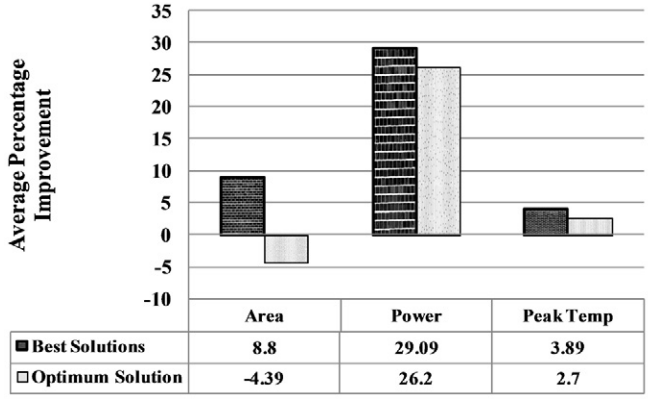

Fig. 12. Average percentage savings of the proposed approach w.r.t. AIGs circuit decomposition [37].

TABLE VI. Post Layout Analysis Of Floorplan Area (μm²), Power (nW), and Temperature (°C)

Circuits	Proposed MPRM						SRMDD [22]				Espresso decomposed AIGs structure [37]			Max. CPU Time (s)
	Best solutions			Optimum solution			Best solutions		Optimum solution					
	Area (μm²)	Power (nW)	Peak Temp (°C)	Area (μm²)	Power (nW)	Peak Temp (°C)	Area (μm²)	Peak Temp (°C)	Area (μm²)	Peak Temp (°C)	Area (μm²)	Power (nW)	Peak Temp (°C)	
5xp1	145	1264.55	65.21	145	1264.55	65.21	559.88	76.70	559.88	82.12	91.31	1222.25	68.73	0.72
9sym	54.04	1121.23	67.95	89.94	1134.23	68.95	-	-	-	-	56.28	1223.30	72.29	0.60
alu2	250.34	2290.73	67.37	380.98	1942.06	69.27	2583.16	64.05	2583.16	72.57	289.67	2737.17	67.66	0.57
alu4	533.86	5093.27	66.22	676.47	5241.93	66.53	-	-	-	-	798.23	8104.59	71.06	0.89
clip	176.47	1364.12	67.90	176.47	1364.12	67.90	229.73	77.86	229.73	77.86	136.10	1385.40	70.50	0.64
cm162a	56.43	371.48	66.61	56.43	403.24	68.54	119.75	74.63	143.04	82.65	28.04	389.73	66.54	0.46
cm163a	35.91	187.24	62.95	35.91	209.69	63.41	169.65	73.98	179.83	78.91	27.92	294.60	64.50	0.40
con1	13.34	106.98	66.17	17.10	106.98	66.67	-	-	-	-	15.17	185.60	66.32	0.36
cu	9.23	88.91	63.81	14.12	88.91	65.32	-	-	-	-	24.26	186.45	65.17	0.31
inc	96.78	862.40	64.60	114.57	862.40	65.75	543.04	67.93	559.81	80.44	82.42	835.20	67.18	0.65
misex1	25.39	313.81	63.54	32.16	459.74	63.94	239.71	73.02	276.51	77.66	43.44	496.53	65.38	0.40
misex2	29.41	199.20	63.47	29.41	199.20	63.47	-	-	-	-	71.82	432.52	62.66	0.40
misex3c	285.57	1324.64	66.50	389.88	1631.50	68.15	-	-	-	-	406.30	3986.98	72.10	0.68
pm1	9.23	82.67	62.33	11.63	82.67	62.70	-	-	-	-	32.49	337.15	65.22	0.30
rd53	20.86	346.28	66.72	20.86	346.28	66.72	149.87	84.90	149.87	89.32	29.46	460.21	69.05	0.36
rd73	40.96	598.21	68.92	40.96	598.21	68.92	446.57	78.41	446.57	78.41	49.11	897.40	73.24	0.52
rd84	57.45	736.43	69.42	57.45	736.43	69.42	-	-	-	-	72.60	910.60	76.22	0.56
sao2	98.49	963.07	65.72	98.49	963.07	67.14	-	-	-	-	102.40	1094.18	68.53	0.62
table3	728.12	2343.71	65.67	771.55	2390.37	67.40	-	-	-	-	734.24	2843.53	69.10	1.00
x2	27.70	170.46	62.27	32.83	214.61	64.02	166.53	96.57	166.53	73.42	32.15	337.74	66.42	0.41
Average % savings w.r.t. SRMDD best solutions [22]	**75.21**		**13.52**	**73.69**		**12.49**								
Average % savings w.r.t. SRMDD optimum solutions [22]	**76.20**		**17.06**	**74.82**		**16.08**								
Average % savings w.r.t. AIGs Circuits [37]	**8.80**	**29.09**	**3.89**	**-4.39**	**26.20**	**2.70**								

VI. Conclusion and Future Works

This paper proposed an NSGA-II based input variable polarity selection of MPRM expansion for thermal aware realization. Area, power, and temperature are considered simultaneously as objective parameters. Product terms are considered as representative area, and switching activity is considered as the power consumption at logic level. Power per unit area (Power density) is taken as the temperature metric to estimate the effect of temperature. The input polarity of MPRM is chosen such that all the parameters are optimum. To find the non-dominated optimal solution based on input polarity of MPRM circuits, NSGA-II based approach is performed and Pareto optimal solution set is reported.

The proposed results are compared with FPRM, GA based FPRM, SRMDD, MPRM and AIGs based solutions; and significant reduction in area, power and power density generation is observed. Finally, NSGA-II based solutions are implemented using CADENCE tool at 45nm technology to obtain on-chip silicon area and power consumption. The floorplan information and power profile are used to get the absolute temperature generated by a particular logic circuit in degree Celsius using HotSpot tool. Maximum 76.20% saving in area, 29.09% saving in power and 17.06% reduction in peak temperature are observed using the proposed MPRM approach with respect to earlier reported works.

The future research is aimed to figure out the correlation between the ageing aware with the thermal aware design and to find an optimum solution to realize a circuit using MPRM expansion.

Acknowledgment

This work was supported by SMDP-C2SD project sponsored by Ministry of Electronics and Information Technology (Meity), Govt. of India.

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