IMPLEMENTATION OF POWER-EFFICIENT CONTROL UNIT ON ULTRA-SCALE FPGA FOR GREEN COMMUNICATION

Bishwajeet Pandey
Centre of Energy Excellence, Gyancity Research Labs.
Motihari, (India).
E-mail: gyancity@gyancity.com ORCID: https://orcid.org/0000-0001-9674-3586

Keshav Kumar
Centre of Energy Excellence, Gyancity Research Labs.
Motihari, (India).
E-mail: keshav@gyancity.com ORCID: https://orcid.org/0000-0002-2310-5468

Aiza Batool
Sapienza University of Rome.
Rome, (Italy).
E-mail: aizabatooll@gmail.com ORCID: https://orcid.org/0000-0001-5650-3609

Shabeer Ahmad
Gran Sasso Science Institute.
L'aquila, (Italy).
E-mail: shabeer.ahmad@gssi.it ORCID: https://orcid.org/0000-0002-2951-2259

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ABSTRACT

Whole world is suffering from the problem of the energy crisis. This is happening because of the enormous growth of population and industries across the globe. Therefore the whole world is looking to adopt the concepts of green communication technologies and power/energy efficient devices. This work is just towards these technologies. In this work, a power-efficient Control Unit (CU) is designed and implemented on Kintex-7 Ultrascale FPGA. The simulation and power analysis of the control unit is done on VIVADO HLx Design Suite. The power analysis of control unit is observed for different frequency values and it is observed that as the frequency increases the total power consumption also increases. Hence the control unit is more suitable to operate at low frequency values in order to minimize the power consumption. Also, there is a 36% saving in total power consumption when we scale down the device operating frequency of the control unit from 5 GHz to 100 MHz.

KEYWORDS

FPGA, Control Unit, Green Communication, Power Analysis, VIVADO.

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1. INTRODUCTION

The rapid extent of the population and the evolution of industrialization across the globe have led to several problems for the shortage of the Earth's natural resources (Mahapatra *et al.,* 2015; Pietrosemoli & Rodríguez-Monroy, 2019). Therefore people are getting more concerned about saving these resources for the future generation. This can be accomplished using green communication technologies and energy/ power-efficient devices (Kumar, Pandey, & Mohamed, 2019a; Kumar *et al.,* 2019b).

This work is a step towards the idea to promote the technologies of green communication and energy/ power-efficient devices. In this work, a Control Unit (CU) is implemented on FPGA to minimize the power consumption. With the help of various Low Voltage CMOS (LVCMOS) technology, Input/ output (I/O) standards researchers have designed a power-efficient CU on Artix-7 FPGA (Kumar, Pandey, & Hussain, 2019c).

I/O standards are used to minimize power consumption by matching the input and output impedance. A power-efficient CU is designed by authors on Artix-7 FPGA by changing its frequency values. With the change in frequency values the power consumption of the CU with FPGA device changes (Kumar *et al.,* 2019d). Stub Series Terminated Logic (SSTL) I/O Standards are used by researchers to improve the power consumption of CU on 40 nm Virtex-6 FPGA. SSTL I/O standards match the impedance of input load w.r.t to the output load, so that power consumption gets reduced (Chaturvedi, Kaushik, & Baggan, 2019).

An electronic CU is designed by authors on FPGA for controlling the vehicles' system. The Reduced Instruction Set Computer (RISC) Machine (ARM) processor is used along with FPGA for computing parallel tasks (Pérez *et al.,* 2019). To promote the ideas of green communication researchers have implemented a power-efficient CU on Virtex and Spartan family's FPGA (Pandey, 2020). An energy-efficient CU is designed by authors with the help of HSTL and HSUL I/O standard for green communication on 28nm Artix-7 FPGA devices (Kumar, Pandey, & Chaturvedi, 2019e). An energy-

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efficient instruction register is designed by authors for integrating the green communication on Virtex 4, Virtex 5, and Virtex 6 FPGA (Siddiquee *et al.,* 2019). Therefore it has been observed that a lot of work has been done for incorporating the ideas of green communication and energy/power-efficient devices for future generation on CU with various FPGAs, but there is no such work is done on implementing the CU circuit on Kintex-7 ultrascale FPGA, hence in this work, the CU circuit is being designed on Kintex-7 ultrascale FPGA for promoting the techniques of green communication.

2. METHODOLOGY

The implementation setup for CU is done on the Ultra scale Kintex-7 FPGA board. The platform used for simulation of CU on the FPGA board is the VIVADO HLx design suite (Kumar *et al.*, 2019f). For implementing CU on Ultra scale Kintex-7 FPGA board, the FPGA resources utilized are such as Lookup Tables (LUTs), Flip-flops (FF), Input-Output (IO), and Global Buffers (BUFGs) which are shown in Table 1 and Figure 1.

Table 1. FPGA resource utilization for implementing CU.

RESOURCE	UTILIZATION	AVAILABLE	UTILIZATION %
LUT	14	203128	0.01
FF	4	406256	0.01
IO	23	312	7.37
BUFG	1	480	0.21

Source: own elaboration.

The utilization of LUTs are 14 whereas 203128 LUTs are available on FPGA boards for designing CU. Similarly, the utilization FF, IO, and BUFG are 4, 23, and 1 respectively for designing CU on the ultrascale Kintex-7 FPGA.

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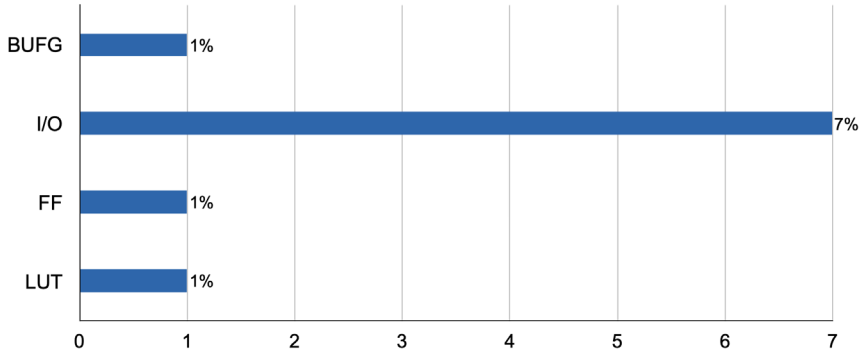

Figure 1. FPGA resource utilization for implementing CU.

Source: own elaboration.

The power analysis of CU for making it energy/power-efficient is done for various frequency values such as 100MHz, 500MHz, 1GHz, 3GHz, and GHz which is shown in Figure 2.

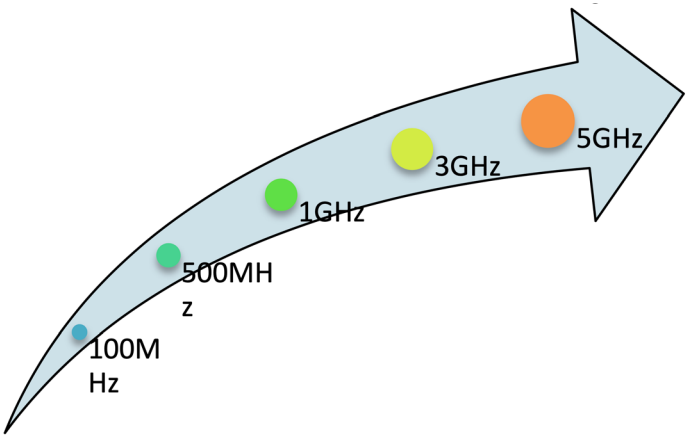

Figure 2. Frequency Values for Power Analysis.

Source: own elaboration.

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3. RESULTS

The power calculation of CU with the ultrascale Kintex-7 FPGA is associated with FPGA device Dynamic Power (DP) and Static Power (SP) (Pandey, 2019). The total power consumption is the sum of both dynamic and static power. The dynamic power is the leakage power dissipation of the device. The static power is the summation of device I/O, Logic (L/G), Signal (S/G), and Clock (Ck) power.

$$Total\ Power\ (TP)=DP+SP$$

3.1. POWER ANALYSIS OF 100 MHZ FREQUENCY

When the frequency of CU is set to 100 MHz then the power consumption is 99% for SP that is 0.457 W and DP consumption is 1% that is 0.007 W. Therefore the device TP consumption is 0.464 W. The TP at 100 MHz is represented in Figure 3.

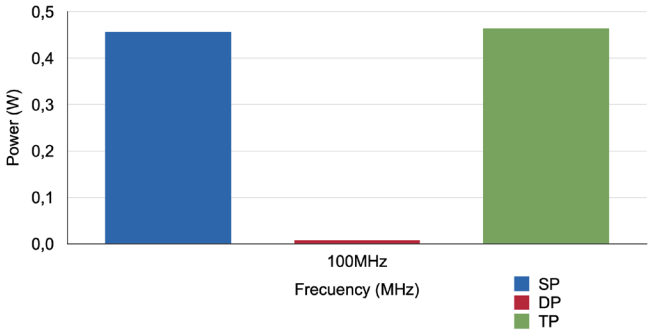

Figure 3. Power Consumption for 100 MHz.

Source: own elaboration.

3.2. POWER ANALYSIS OF 500 MHZ FREQUENCY

When the frequency is tuned to 500 MHz, the total power consumption of CU on the FPGA board is 0.485 W. The TP consumption is the summation of device SP and DP. For the frequency of 500 MHz,

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the SP consumption is 0.457 W whereas DP consumption is 0.028 W. The power consumption for the frequency of 500 MHz is described in Figure 4.

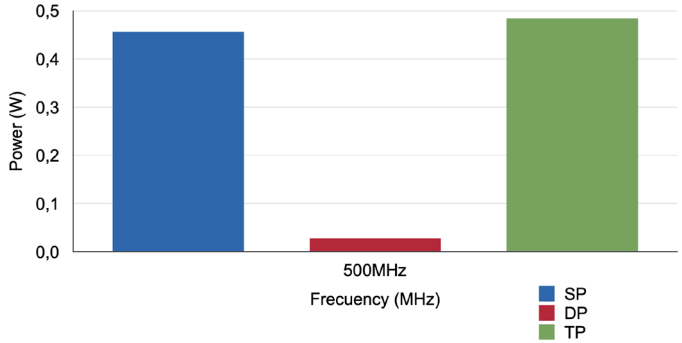

Figure 4. Power Consumption for 500 MHz.

Source: own elaboration.

3.3. POWER ANALYSIS OF 1 GHZ FREQUENCY

When the frequency of CU is tuned to 1 GHz then the power consumption is 89% for SP that is 0.457W and DP consumption is 11% that is 0.054W. Therefore the device TP consumption is 0.512 W. The TP at 100MHz is represented in Figure 5.

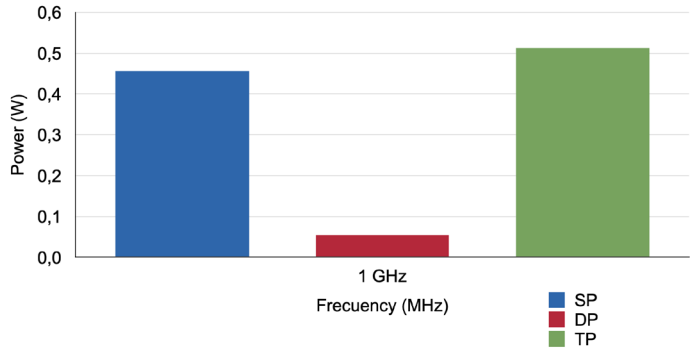

Figure 5. Power Consumption for 1 GHz.

Source: own elaboration.

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3.4. POWER ANALYSIS OF 3 GHZ FREQUENCY

When the frequency is tuned to 3 GHz, the total power consumption of CU on the FPGA board is 0.618 W. The TP consumption is the summation of device SP and DP. For the frequency of 3 GHz, the SP consumption is 0.458 W whereas DP consumption is 0.160 W. The power consumption for the frequency of 3 GHz is described in Figure 6.

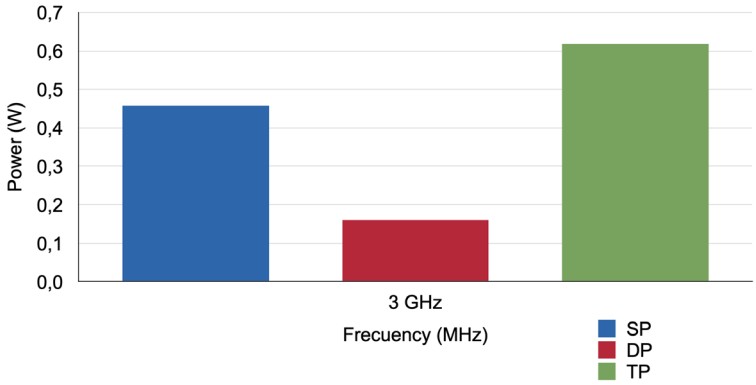

Figure 6. Power Consumption for 3 GHz.

Source: own elaboration.

3.5. POWER ANALYSIS OF 5 GHZ FREQUENCY

When the frequency is tuned to 5 GHz, the total power consumption of CU on the FPGA board is 0.725 W. The TP consumption is the summation of device SP and DP. For the frequency of 5 GHz, the SP consumption is 0.459 W whereas DP consumption is 0.266 W. The power consumption for the frequency of 5 GHz is described in Figure 7.

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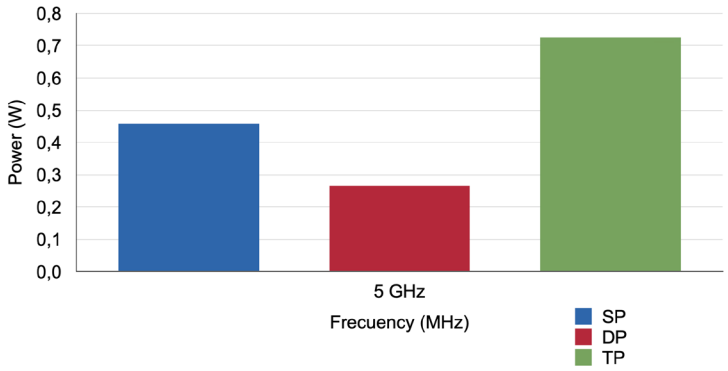

Figure 7. Power Consumption for 5 GHz.

Source: own elaboration.

4. OBSERVATIONS AND DISCUSSION

From the power analysis (section), it is being observed that as the frequency of operation of FPGA devices gets increased there is decrement in the SP of device for CU implementation and there is an increment if device DP for CU implementation. Therefore the TP gets increased, when the frequency gets increased.

The TP consumption is found minimum for 100 MHz frequency whereas the TP consumption is found maximum for 5 GHz frequency. There is an increment of 4.52% in TP consumption, when the frequency value is tuned to 500 MHz from 100 MHz. Also, there is an increment of 10.34 %, 33.18%, and 56.25% in TP consumption, when the frequency value is tuned to 1 GHz, 3 GHz, and 5 GHz from 100 MHz. The total power of the control unit on an FPGA device for all frequency values are shown in Figure 8.

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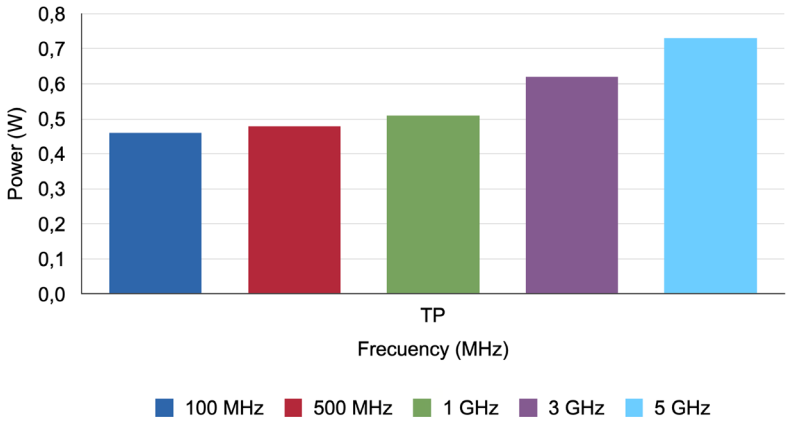

Figure 8. Total Power Consumption of CU on FPGA device.

Source: own elaboration.

5. CONCLUSION AND FUTURE SCOPE

The step towards green communication is very important in this era, because energy crisis is seen everywhere across the globe. Therefore from this research work, it has been tried to make some steps towards promoting the principles of green communication and power-efficient devices. In this work, the implementation of CU is done on Kintex-7 ultrascale FPGA, and the simulation of CU circuit, resources utilization, and power analysis is observed on VIVADO Hlx Design Suite.

The power consumption of CU on FPGA devices is analyzed for five different sets of frequency values such as 100 MHz, 500 MHz, 1 GHz, 3 GHz, and 5 GHz. It is observed that the power consumption increases as the value of frequency increases. Therefore it can be concluded that lower the frequency value lower the total power consumption. The CU circuit consumes the least amount of power for 100 MHz frequency.

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As future scope is concerned, this CU circuit can be analyzed for other ultra-scale and ultrascale plus FPGA devices. Not only this other power-efficient techniques such as voltage, current, and capacitance scaling techniques can be applied to the CU circuit. Impedance matching techniques with the help of I/O standards can also be applied to make circuit energy-efficient. Later this FPGA design can be converted to ASIC designs for better performance.

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