ENERGY EFFICIENT AND HIGH–PERFORMANCE FIR FILTER DESIGN ON SPARTAN–6 FPGA

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ABSTRACT

In this paper, we are going to design the energy efficient Gaussian low pass FIR filter on spartan–6 FPGA. To make an energy efficient filter, we have used different methods in this paper like capacitance scaling, frequency scaling, and then we analysed the demand for power by Gaussian low pass FIR filter. The frequency range which is used in this paper is 1 GHz, 2GHz, 2.5GHz, 5 GHz, 10 GHz and the range of capacitance which we have used in this paper is 5pF, 10pF, 25pF, 40pF and 50 pF. An FIR filter always remnants in linear phase with the help of symmetric coefficient and this is the very useful feature of the FIR filter for phase sensitive application like data communications etc. At present, there are many different methods of communications and networking. So, in this paper, we have designed an energy–efficient FIR filter and that design will faster than traditional design.

KEYWORDS

FIR filter, Gaussian, FPGA, Energy efficient, Spartan–6 FPGA.

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1. INTRODUCTION

Gaussian filter is a type of filter and the impulse response of this filter is in Gaussian function. A linear phase is the important feature of any filter. Linear phase means that the filter phase response of the filter will be a linear function of frequency. A finite impulse response (FIR) is a filter and it settles to zero in finite time so then impulse response, and that features make the FIR an ideal choice for phase sensitive application i.e. data communications, seismology, crossover filters and mastering etc. Here we can say that an energy efficient design of FIR filter leads to energy efficient data communication.

Figure 1. Top Level Schematic of Gaussian Low Pass FIR Filter.

Spartan–6 FPGA is a high–performance FPGA in terms of price and performance using 45nm transistor technology. The function of the low pass filter is to pass the low–frequency signals and prohibits the signals which are higher than the cut–off frequency as shown in Figure 1. In this paper, we have operated the Gaussian low pass filter with 1GHz, 2GHz, 2.5GHz, 5GHz, and maximum of 10 GHz frequency. We have also used capacitance scaling method to analyse the power (Pandey, Kumar, Das, Yadav & Pandey, 2014).

2. LITERATURE SURVEY

In Pandey, *et al.* (2014), the author has used capacitance scaling techniques as well as frequency scaling techniques but on 28nm Kintex–7 FPGA using available 240 DSP slice. There is open scope to design different energy efficient DSP IP block like Modulation, Transforms, Tring functions, Demodulation, Error

Correction. In this paper, the dynamic power of the CMOS circuit is dependent on the capacitance of payload and switching activity of circuit. Due to the operating frequency of the device is high, the clock signal is the main factor for the generation of dynamic power. The paper of Pandey, *et al.* (2014) shows that there are no change in DSP power, signal power, logic power if there is a change in capacitance, but IO power and leakage power are increasing so the overall power is also increasing. In Pandey, Kumar, Das, Islam and Kumar (2014) the authors analyse that there is no any change in clock power due to airflow, but the airflow is affecting the logic power, signal power, DSPs power and IOs power and they are increasing. The authors have used 250 LFM and 500LFM airflow in order to design an energy efficient FIR filter. They have used custom, low profile, medium profile and high profile hit the sink. In Pandey, *et al.* (2018), FIR filter is using 5% of IO resource available in ultra–scale FPGA. So, then there is a possibility to implement bigger FIR filter in this ultra–scale FPGA. FIR filter is using 1 out of 480 clock buffer available on FPGA so then it provides 479 remaining global clock buffer to the different component of future design. The distribution of dynamic and static power is 15% and 85% as shown in Figure 2.

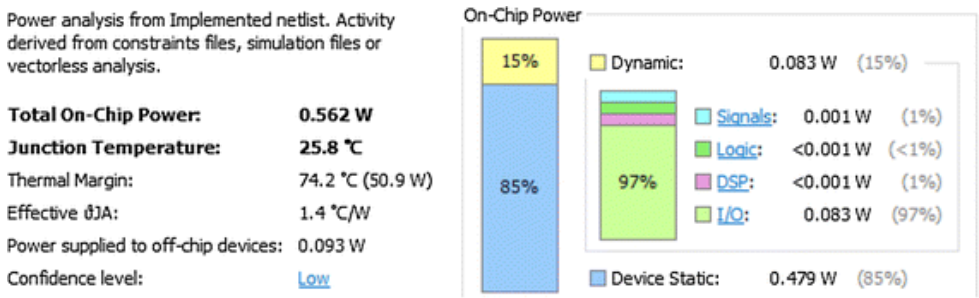

Figure 2. Power Dissipation of FIR Filter. **Source:** Pandey, *et al.*, 2018.

In Pandey, *et al.* (2017), the author has analysed the power demand by device of Artix–7, Kintex–7, Zynq and ultrascale FPGA then they conclude that all programmable SoC is a power hungry architecture but Kintex ultra–scale architecture is the very energy efficient architecture. There is significant improvement when they migrate design from 28 nm process technology based seven series architecture to 20 nm process technology based ultra–scale architecture. Reduction in latency will increase the efficiency of any communication design

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not only this FIR Filter but also many others. The requirement for accurate, high performance and indoor localization using wireless sensor networks (WSNs) is increasing day by day (Pak, Ahn, Shmaliy & Lim, 2015). Zhao, Shmaliy, Huang and Liu (2015) research work is concerned with the minimum variance unbiased (MVU) finite impulse response (FIR) filtering problem for a linear system. Digital filters are mainly used in a lot of digital signal processing areas. Filters of finite impulse response (FIR) category has stability and compliance to be adaptive, in compare to filters of infinite impulse response (IIR) category (Mirghani, 2018). Transpose form finite–impulse–response (FIR) filters are inherently pipelined and support multiple constant multiplications (MCM) technique (Mohanty & Meher, 2016).

3. RESULT AND DISCUSSION

Table 1 has shown the total power consumption of Gaussian low pass FIR filter for 5 pF capacitance at different frequencies. The total power consumption in Gaussian low pass FIR filter for 5 pF capacitance is 0.072W, 0.125W, 0.153W, 0.291W, 0.566W on 1 GHz, 2 GHz, 2.5 GHz, 5 GHz, 10 GHz respectively.

Table 1. Power of Gaussian Low Pass FIR Filter for 5 pF Capacitance.

Frequency	Dynamic Power (Watt)	IO–Power (Watt)	Leakage Power (Watt)	Total Power (Watt)
1 GHz	0.017	0.040	0.015	0.072
2 GHz	0.029	0.081	0.015	0.125
2.5 GHz	0.036	0.101	0.016	0.153
5 GHz	0.074	0.201	0.017	0.291
10 GHz	0.144	0.403	0.020	0.566

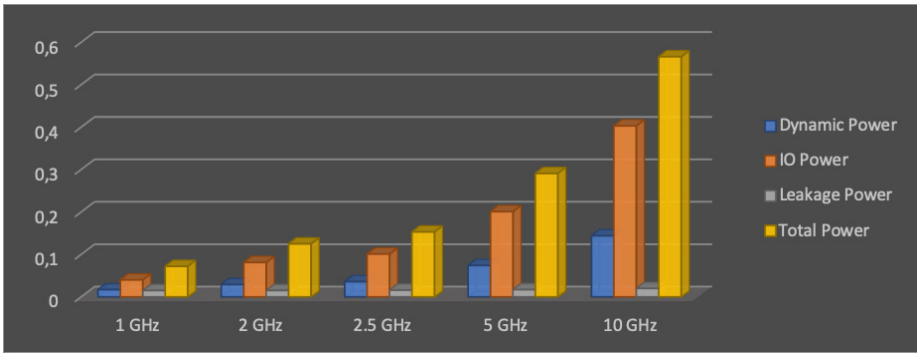

Figure 3. Power Dissipation of GLP FIR Filter on a different frequency and 5 pF capacitance.

As we can see, power dissipation is increasing with respect to frequency and capacitance. The total power is the sum of static and dynamic power, and the Dynamic Power is the sum of signal, clock, and logic power. The distribution of power analysis has shown in Figure 3.

Table 2. Power of Gaussian Low Pass FIR Filter for 10 pF Capacitance.

Frequency	Dynamic Power (Watt)	IO–Power (Watt)	Leakage Power (Watt)	Total Power (Watt)
1 GHz	0.017	0.049	0.015	0.080
2 GHz	0.029	0.097	0.016	0.142
2.5 GHz	0.036	0.121	0.016	0.174
5 GHz	0.074	0.242	0.017	0.333
10 GHz	0.144	0.485	0.021	0.650

Table 2 has shown the total power consumption of Gaussian low pass FIR filter for 10 pF capacitance at different frequencies. The total power consumption in Gaussian low pass FIR filter for 10 pF capacitance is 0.080W, 0.142W, 0.174W, 0.333W, 0.650W on 1 GHz, 2 GHz, 2.5 GHz, 5 GHz, 10 GHz respectively. So, we can conclude that the total power is increasing with respect to frequency and capacitance. The total power is the sum of static and dynamic power, and the Dynamic Power is the sum of signal, clock, and logic power as shown in Figure 4.

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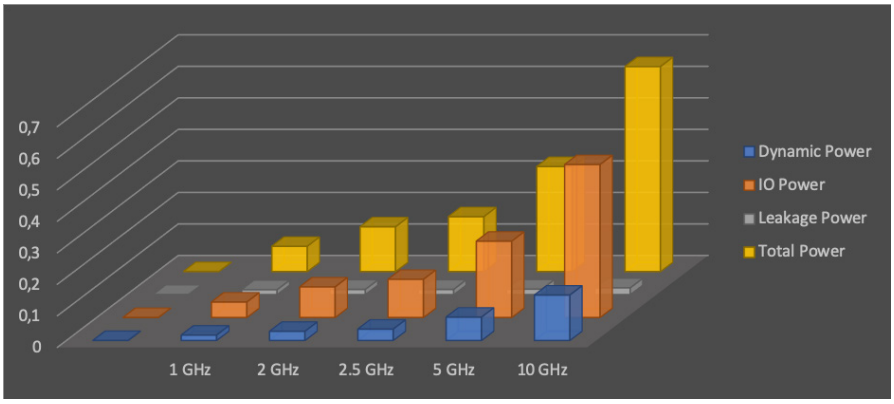

Figure 4. Power Dissipation of GLP FIR Filter on a different frequency and 10 pF capacitance.

Table 3. Power of Gaussian Low Pass FIR Filter for 25 pF Capacitance.

Frequency	Dynamic Power (Watt)	IO–Power (Watt)	Leakage Power (Watt)	Total Power (Watt)
1 GHz	0.017	0.073	0.015	0.105
2 GHz	0.029	0.146	0.016	0.192
2.5 GHz	0.036	0.183	0.016	0.236
5 GHz	0.074	0.366	0.019	0.458
10 GHz	0.144	0.731	0.025	0.900

Table 3 has shown the total power consumption of Gaussian low pass FIR filter for 25 pF capacitance at different frequencies. The total power consumption in Gaussian low pass FIR filter for 25 pF capacitance is 0.105W, 0.192W, 0.236W, 0.458W, 0.900W on 1 GHz, 2 GHz, 2.5 GHz, 5 GHz, 10 GHz respectively. IO–Power is the major contributor in total power dissipation of the FIR filter as shown in Figure 5.

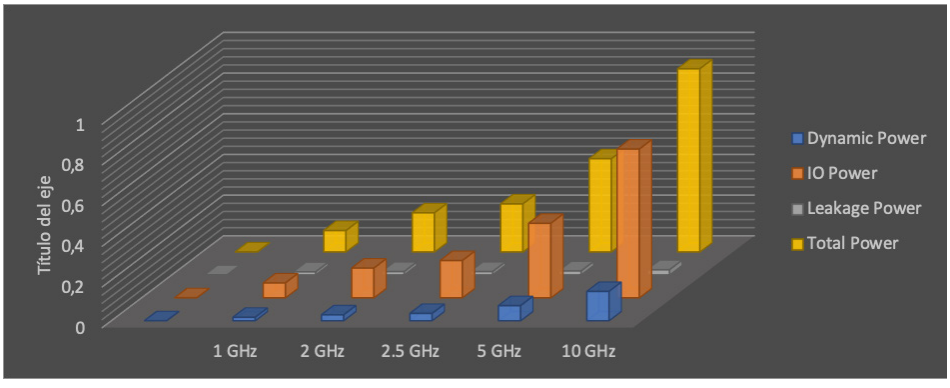

Figure 5. Power Dissipation of GLP FIR Filter on different frequencies and 25 pF capacitance.

Table 4. Power of Gaussian Low Pass FIR Filter for 40 pF Capacitance.

Frequency	Dynamic Power (Watt)	IO–Power (Watt)	Leakage Power (Watt)	Total Power (Watt)
1 GHz	0.017	0.098	0.015	0.130
2 GHz	0.029	0.196	0.017	0.241
2.5 GHz	0.036	0.244	0.017	0.298
5 GHz	0.074	0.489	0.020	0.582
10 GHz	0.144	0.978	0.030	1.151

Table 4 has shown the total power consumption of Gaussian low pass FIR filter for 40 pF capacitance at different frequencies. The total power consumption in Gaussian low pass FIR filter for 40 pF capacitance is 0.130W, 0.241W, 0.298W, 0.582W, 1.151W on 1 GHz, 2 GHz, 2.5 GHz, 5 GHz, 10 GHz respectively. So, dynamic power is approx. 13% of total power dissipation and static power is 87% of total power dissipation for 1 GHz as shown in Figure 6.

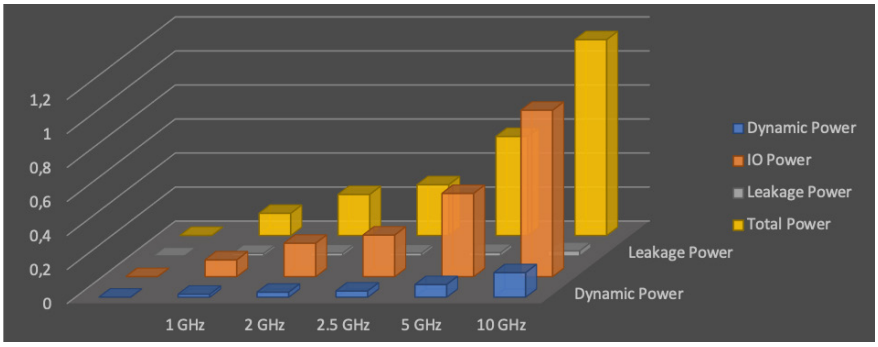

Figure 6. Power Dissipation of GLP FIR Filter on different frequencies and 40 pF capacitance.

Table 5. Power of Gaussian Low Pass FIR Filter for 50 pF Capacitance.

Frequency	Dynamic Power (Watt)	IO–Power (Watt)	Leakage Power (Watt)	Total Power (Watt)
1 GHz	0.017	0.114	0.016	0.147
2 GHz	0.029	0.228	0.017	0.275
2.5 GHz	0.036	0.286	0.018	0.340
5 GHz	0.074	0.571	0.022	0.666
10 GHz	0.144	1.142	0.034	1.320

Table 5 has shown the total power consumption of Gaussian low pass FIR filter for 50 pF capacitance at different frequencies. The total power consumption in Gaussian low pass FIR filter for 50 pF capacitance is 0.147 W, 0.275 W, 0.340 W, 0.666 W, 1.320 W on 1 GHz, 2 GHz, 2.5 GHz, 5 GHz, 10 GHz respectively. So, we can say that dynamic power is increasing with respect to frequency. The total power is the sum of static and dynamic power as shown in Figure 7.

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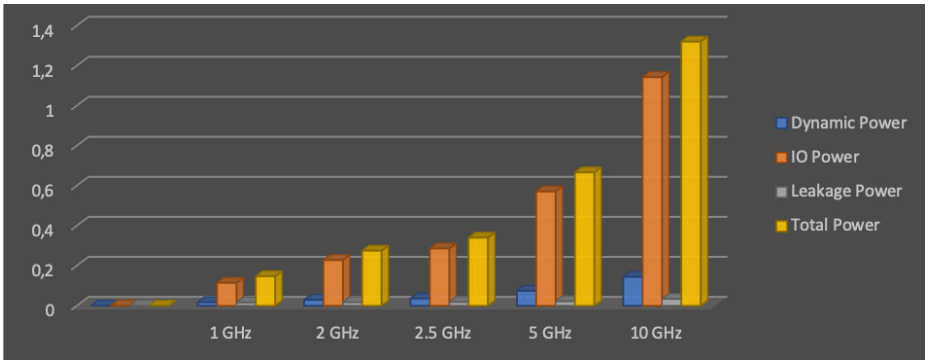

Figure 7. Power Dissipation of GLP FIR Filter on a different frequency and 40 pF capacitance.

Table 6. IO Power analysis of Gaussian Low Pass FIR Filter.

Frequency	5 pF	10 pF	25 pF	40 pF	50 pF
1 GHz	0.040	0.049	0.073	0.098	0.114
2 GHz	0.081	0.097	0.146	0.196	0.228
2.5 GHz	0.101	0.121	0.183	0.244	0.286
5 GHz	0.201	0.242	0.366	0.489	0.571
10 GHz	0.403	0.485	0.731	0.978	1.142

As we can see in Table 6, the IOs power is decreasing by decreasing the device operating frequency and by decreasing the capacitance values. It is decreasing at approx. 14%, 35%, 57%, 64% when the capacitance value is scaled down from 50 pF to 40pF, 25pF, 10pF and 5 pF for the all range of frequency, which we have used for FIR filter i.e. 1 GHz, 2 GHz, 2.5 GHz, 5 GHz, 10 GHz. In another way, the IOs power is decreasing by 50%, 75%, 80%, 90% when we decrease the FIR filter device operating frequency from 10 GHz to 5 GHz, 2.5GHz, 2 GHz and 1 GHz for all capacitance values as shown in Figure 8.

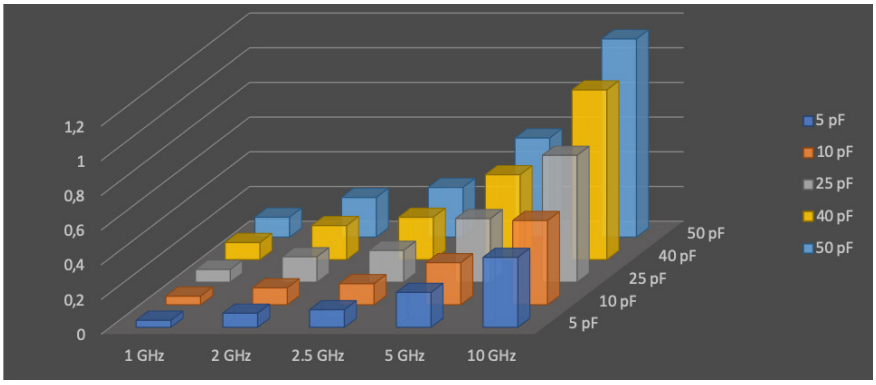

Figure 8. IO–Power Dissipation of GLP FIR Filter on the different capacitance value.

Table 7. Leakage Power analysis of Gaussian Low Pass FIR Filter.

Frequency	5 pF	10 pF	25 pF	40 pF	50 pF
1 GHz	0.015	0.015	0.015	0.015	0.016
2 GHz	0.015	0.016	0.016	0.017	0.017
2.5 GHz	0.016	0.016	0.016	0.017	0.018
5 GHz	0.017	0.017	0.019	0.020	0.022
10 GHz	0.020	0.021	0.025	0.030	0.034

As we can see in Table 7, the Leakage power is decreasing by decreasing the device operating frequency and by decreasing the capacitance values. It is decreasing at approx. 6%, 12%, 20% when the capacitance value is scaled down from 50 pF to 5 pF for 2 GHz to 10 GHz frequency. In another way, the leakage power is decreasing by 25%, 28%, 40%, 50% and 52% when we decrease the FIR filter device operating frequency from 10 GHz to 1 GHz for 5 pF, 10 pF, 25 pF, 40 pF, 50 pF capacitance value respectively. This analysis has shown in Figure 9.

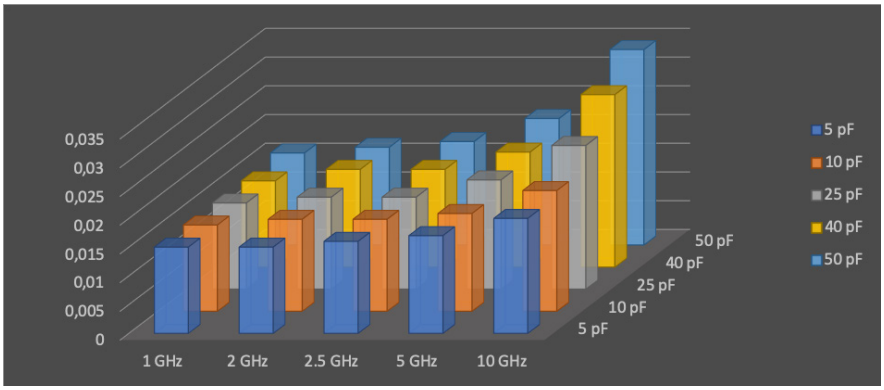

Figure 9. IO–Power Dissipation of GLP FIR Filter on the different capacitance value.

Table 8. Total Power analysis of Gaussian Low Pass FIR Filter.

Frequency	5 pF	10 pF	25 pF	40 pF	50 pF
1 GHz	0.072	0.080	0.105	0.130	0.147
2 GHz	0.125	0.142	0.192	0.241	0.275
2.5 GHz	0.153	0.174	0.236	0.298	0.340
5 GHz	0.291	0.333	0.458	0.582	0.666
10 GHz	0.566	0.650	0.900	1.151	1.320

As we can see in Table 8, the total power is decreasing by decreasing the device operating frequency and by decreasing the capacitance values. It is decreasing at approx. 12%, 30%, 48%, 57% when the capacitance value is scale down from 50 pF to 40pF, 25pF, 10pF and 5 pF respectively. In another way, the total power is approx. 88% decreasing when we decrease the FIR filter device operating

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frequency from 10 GHz to 1 GHz as shown in Figure 10.

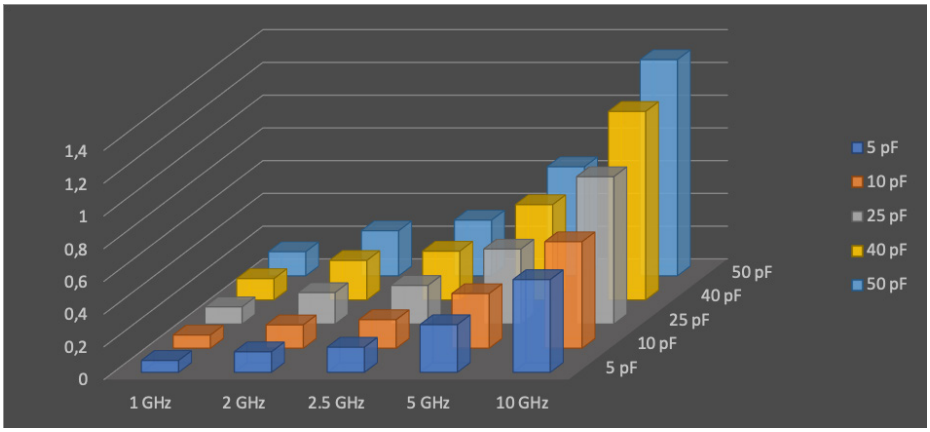

Figure 10. IO–Power Dissipation of GLP FIR Filter on the different capacitance value.

4. CONCLUSION

According to the above analysis, we have analysed dynamic power are increasing due to change in device operating frequency but for the same frequency, the dynamic power remains the same for any value of capacitance. Instead of this, the IO power, leakage power is increasing if we use capacitance scaling techniques as well as scaling of device operating frequency. The IO power is decreasing approx. 14%, 35%, 57%, 64% when the capacitance value is scaled down from 50 pF to 40pF, 25pF, 10pF and 5 pF for the all range of frequency, which we have used for FIR filter i.e. 1 GHz, 2 GHz, 2.5 GHz, 5 GHz, 10 GHz. The leakage power is decreasing approx. 6%, 12%, 20% when the capacitance value is scaled down from 50 pF to 5 pF for 2 GHz to 10 GHz frequency. But here we can say that the leakage power is increasing very slowly with increasing capacitance. The total power is decreasing approx. 12%, 30%, 48%, 57% when the capacitance value is scale down from 50 pF to 40pF, 25pF, 10pF and 5 pF respectively. In another way, the total power is 88% and 50% decreasing when we decrease the FIR filter device operating frequency from 10 GHz to 1 GHz and 5 GHz respectively.

5. FUTURE SCOPE

In this paper, we have used the Spartan–6 FPGA to design the energy efficient Gaussian low pass filter. There are many open scopes available to make the energy efficient filter design using Floating–Point, Modulation, Transforms, Demodulation, Video, Error Correction, Imaging and even more DSP IP block. The current FPGA which we have used in this paper is 45nm FPGA. There is open scope to implement the design on 28nm FPGA, 20nm or even lower 14nm ultra–scale FPGA.

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