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DESIGN OF AN OPERATIONAL AMPLIFIER USING DIFFERENTIAL EVOLUTION ALGORITHM

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Resumen: Hoy en día, uno de los parámetros más importantes para el diseño de circuitos integrados es elegir el adecuado de longitud y ancho de transistor en el proceso CMOS. El propósito de este trabajo es utilizar un algoritmo de evolución diferencial para optimizar los parámetros del amplificador operacional. El circuito utiliza una técnica de optimización multiobjetivo para optimizar varias características del amplificador tales como ancho de banda, consumo de energía, etc. como los parámetros de la función de coste. En este trabajo, se considera un nuevo método que utiliza un algoritmo genético multiobjetivo basado en el Frente de Pareto para diseñar una estructura cascode telescópica. En este diseño, dos transistores actúan como controladores de entrada y los otros dos transistores actúan como corriente de carga activa, proporcionando una alta resistencia de salida para esta clase. Los transistores utilizados para cascoding transistores de entrada y los transistores de carga activos se utilizan para aumentar la salida del circuito y por lo tanto resultar en una alta ganancia para todo el circuito. El consumo máximo de potencia debe ser de 5 mW, el valor de ganancia es igual a 2143,3 y la tensión de polarización para los transistores es de 1,6 V.

Palabras clave: Circuitos integrados, Algoritmo de evolución diferencial, Optimización, Telescópico, Cascode, Algoritmo genético, Frente de Pareto

Abstract: Today, one of the most important parameters for designing integrated circuits is to choose the suitable of length and width of transistors in CMOS process. The purpose of this paper is to use a differential evolution algorithm to optimize the parameters of operational amplifier. The circuit uses a multi-objective optimization technique to optimize several charactersics of amplifier such as bandwidth, power consumption, etc. as the cost function parameters. In this paper, a new method using multi-objective genetic algorithm based on the Pareto Front for designing the telescopic cascode structure is considered. In this design, two transistors play as input drivers and the other two transistors act as active load current providing high output resistance for this class. Transistors used for cascoding input transistors and active load transistors were used to increase the output of the circuit and thus result in a high gain for the entire circuit. The maximum power consumption should be 5 mW, the gain value was equal to 2143.3 and the bias voltage for transistors was 1.6 V.

Keywords: Integrated Circuits, Differential Evolution Algorithm, Optimization, Telescopic, Cascode, Genetic Algorithm, Pareto Front

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1. INTRODUCTION

The rapid growth of the semiconductor market and the production of integrated circuits in recent years along the introduction of centralized systems on a chip have required the development of analog and digital systems together. Today, the analogue section of complex systems is much smaller than their digital. Nevertheless, the design of the analogue section is more time-consuming than the digital. The reason for this is the design of analog circuits based on the requirements. In many cases, the design requirements are such that no predesigned analog components able to use and the designer has to design analog components in accordance with the requirements. Accordingly, one of the main challenges in designing analog components is to optimize their parameters based on the requirements. In recent years, many studies have been done on the design of analog circuits using evolutionary algorithms, which single-objective functions used in most of these methods; however as we know, analog design is a multi-objective problem and the designer should compromise between different indices such as interest, bandwidth, phase margin, power consumption, chip level, etc. (Nizamuddin, M., et al, 2016).

There are two steps to designing analog circuits. In the first step, the circuit topology has been determined. In the second step, the parameters of the parts used are determined. Obviously, it is important to reduce the power consumption and the speed of the piece in choosing the value of the parameters of the parts used in the design. Operational amplifiers are used in many cases, including integrated circuits, power amplifiers, instrumentation circuits, and ect. Therefore, the optimal design of the operational amplifier is of great importance. Today, the most important challenge in designing integrated circuits is to reduce power consumption, increase speed and reduce its level on semiconductor wafer. Accordingly, a systematic algorithm is proposed for the proper design of operational amplifier by the researchers (Ortega-Torres, E., et al. 2015).

One of the most important parameters in the design of integrated circuits is the correct choice of length and width in transistors used. In the operational amplifier like any integrated circuit, a number of transistors are used to design it on the wafer surface (Ortega-Torres, E., et al. 2015).. The operational amplifier is in fact a very high voltage amplifier and usually has an output terminal and two input terminals that act as differential. In other words, this amplifier boosts the voltage difference between the inputs. One of the two terminals is called a negative or inverting input, because the amplifier for the inputs applied to this terminal will have a negative gain. The other terminal is a positive or non- inverting input, and the input signals to this terminal appear in the output with positive gain. This amplifier has a very small output resistance of a few ohms with very large input resistance of more than a few hundred ohms. Operational amplifiers are direct coupling amplifiers with a very high voltage gain. Therefore, if there is a very small potential difference in inputs, then the output should have a very large voltage, but in practice the amplifier enters the saturation region and acts in a nonlinear manner. If the operational amplifier as a linear amplifier is used, the desired amplification factor of the amplifier will be controlled in different ways. Operational amplifiers have a variety of applications in electronic systems. Operational amplifiers have a variety of applications in the electronic system, economically feasible and inexpensive, with advantages such as small dimensions, high reliability and good thermal stability (Udwadia, F. E. and Trifunac, M. D. 1973). The purpose of this research is to use a differential evolution algorithm to optimize the parameters in the operational amplifier. The design of the operational amplifier circuit in this paper is considered as a multi-objective optimization problem, which has several design goals such as bandwidth, power consumption, etc. as the cost function parameters (Ortega-Torres, E., et al. 2015).

2. PROPOSED METHOD

Most real-life optimization issues are naturally multi-objective, in which they should meet several goals simultaneously. Recent work on evolutionary multi-objective optimization algorithms has been designed to maintain the distribution of responses and implement elitism to maintain the quality of the answers in later generations.

There are two different attitudes in implementing a differential evolutional algorithm for circuit design. In the first approach, the topology of the circuit is constant and the algorithm only provides the values of the circuit elements; however, in the second approach, the topology algorithm changes the circuit and gains the values of the elements. In this research, the first approach is used. The main purpose of this paper is to use a differential

evolution algorithm for designing operational amplifier parameters. The most important feature of the differential evolution algorithm is to calculate the amplifier parameters as a systematic method. In this research, the operational amplifier dynamics will first be obtained and then the design of its parameters will be deployed using a differential evolution algorithm based on the model. In this method, the determination of elements values is done by a differential evolution algorithm, and the designer does not need to do any calculations, and can only determine the range of parameters to increase the convergence of the algorithm.

The purpose of the design is to implement an operational amplifier with a differential input and a single-terminal output with the characteristics of Table 1.

Table 1. Optional Amplifier Parameters

Specifications	Required range
DC gain	**<100000**
Unity gain bandwidth	**100MHz<**
Phase margin	**< 70** ◦
Maximum output swing	**VP-P<2**
Power consumption	As low as possible
Chip level	As low as possible
Vdd	**V2/5**

In order to reach the high gain, a telescopic cascode inlet level has been used and for the maximum amplitude at the output, the second level of a common source with active load is used (Fig. 1).

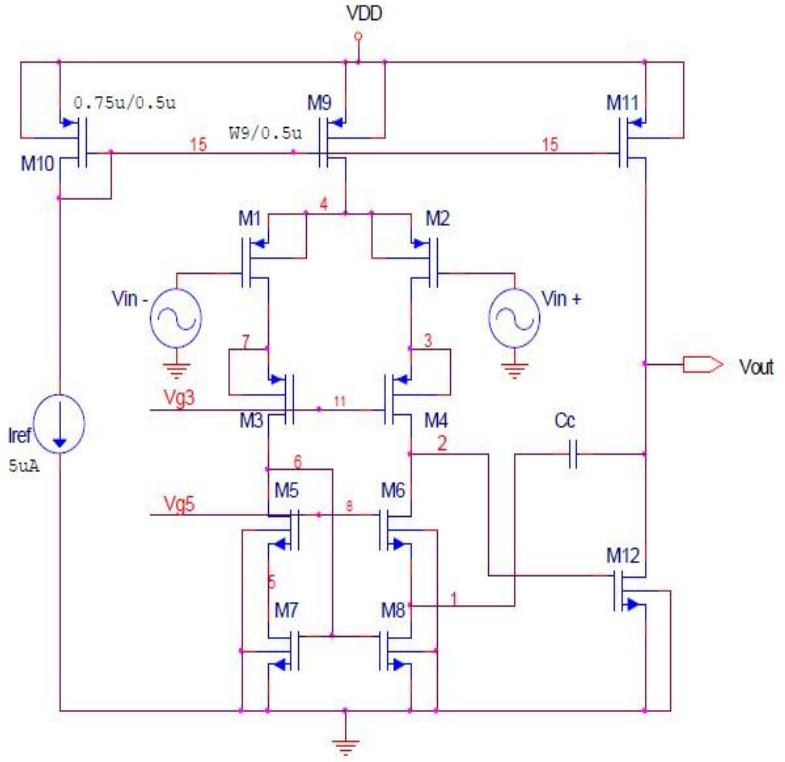

Figure 1. Changes in proposed structure of the desired amplifier

For the above circuit design, the values of Iref, the size of the transistor M10 and the value of L transistor M9 have been considered fixed. The rest of the elements values are including the design parameters of the circuit, which are obtained by differential evolution algorithm.
These parameters are:

- W / L value of transistor M9
- L and W / L values of transistors M1 and M2
- L and W / L values of transistors M3 and M4
- L and W / L values of transistors M5 and M6
- L and W / L values of transistors M7 and M8

The above transistors are two by two identical.

- Vgs Voltages Vg3, Vg5 and Vin
- L and W / L values of transistor M11
- L and W / L values of transistor M12
- Compensator Capacitor value of Cc

To increase the convergence rate of the algorithm, it is appropriate to specify the range of parameters

allowed by the designer. This is especially true for bias voltages because in the implementation of the algorithm after the simulation, it is first checked that all transistors are active in the region; otherwise a large negative response will be given to it to eliminate that answer in subsequent generations. The desired output parameters are: voltage gain, bandwidth, phase margin, power consumption and chip level, which are used as cost functions in differential evolution algorithms.

The use of biased transistors in the empty space in modern digital low voltage technologies is inevitable. Analogue compensation techniques are often in these transistors used to reduce the extreme nonlinear behavior of capacitance and informed to the author of the interface; however, the latest state of the articles can be tracked through the conference website at any moment. If accepted, it is necessary for the authors of the article to apply the amendments requested by the referees in the final version within the time period requested and send the final version through the conference website.

3. PROCESS OF IMPLEMENTING A DIFFERENTIAL EVOLUTION ALGORITHM

Like other population-based optimization algorithms, DE also includes two steps: initialization and evolution. In the initial phase, if there is no information about the problem, the DE population is generated randomly. At the evolution stage, the populations through mutation, recombination and selection process repeatedly have been improved until the algorithm termination criterion is satisfied. Without loss of integrity, one problem is to minimize the function f (x), which is discussed here.

$$\text{Min } f(x) \quad , \quad X=[x_1,x_2,\ldots,x_d] \quad , \quad x_i \in [a_i,b_i] \tag{1}$$

Where f (x) is the target function and X is the decision vector consisting of a variable D. ai and bi represent the upper and lower boundaries of xi, respectively. In the standard DE model, each person represents a candidate solution for f (x) in the search space. In each generation, the objective function is evaluated for each person. The value obtained is used to evaluate the quality of individuals during the optimization process and in order to find the best member (Brest, J., et al. 2006).

In the initial phase, all individuals from entire population are randomly values assigned with a uniform probability distribution in the search space. The main difference between differential evolution algorithm and genetic algorithm is mutation. In the intersection operation, the candidate children vector is produced according to the following equation:

$$u_{ij}^{g}=\begin{cases} v_{ij}^{g} \ , \ rand(j)\le CR \\ \qquad\qquad\qquad\qquad j\in\{1,2,\ldots,D\} \\ x_{ij}^{g} \ , \ rand(j)>CR \end{cases} \tag{2}$$

In which u_{ij}^{g} is a parameter of candidate children vector U_i^g and v_{ij}^{g} a parameter of the V_i^g vector, CR is the intersection rate, which is limited to [0,1]. Mainly two types of binary and exponential intersections are used. The difference between them is in the way they are produced. In the differential evolution algorithm, the CR value is the same for all individuals during evolution, but in comparative differential evolution algorithms, the CR value is different during the evolution process. The final step in implementing the algorithm is the selection stage. This stage is of particular importance and it can be said that selection has the role of a competitive mechanism. The candidate and the old individual compete according to their merit. The winner will have a chance to survive and will be transferred to the next generation, which is calculated from equation (3).

$$X_i^{g+1}=\begin{cases} U_i^g & if \quad f(X_i^g)>f(U_i^g) \\ X_i^g & otherwise \end{cases} \tag{3}$$

DE of mutation processes repeat the intersections, and choices until the termination conditions are satisfied, and the output is a final candidate solution for f (X). The flowchart shows how the differential evolution algorithm works. The corresponding algorithm should determine the proper values of W / L transistors, the transistors optimal dimensions of the compensator capacitive, and ultimately the circuit-bias voltages in the way to optimize the important parameters of the amplifier (power consumption, chip level, and signal processing quality).

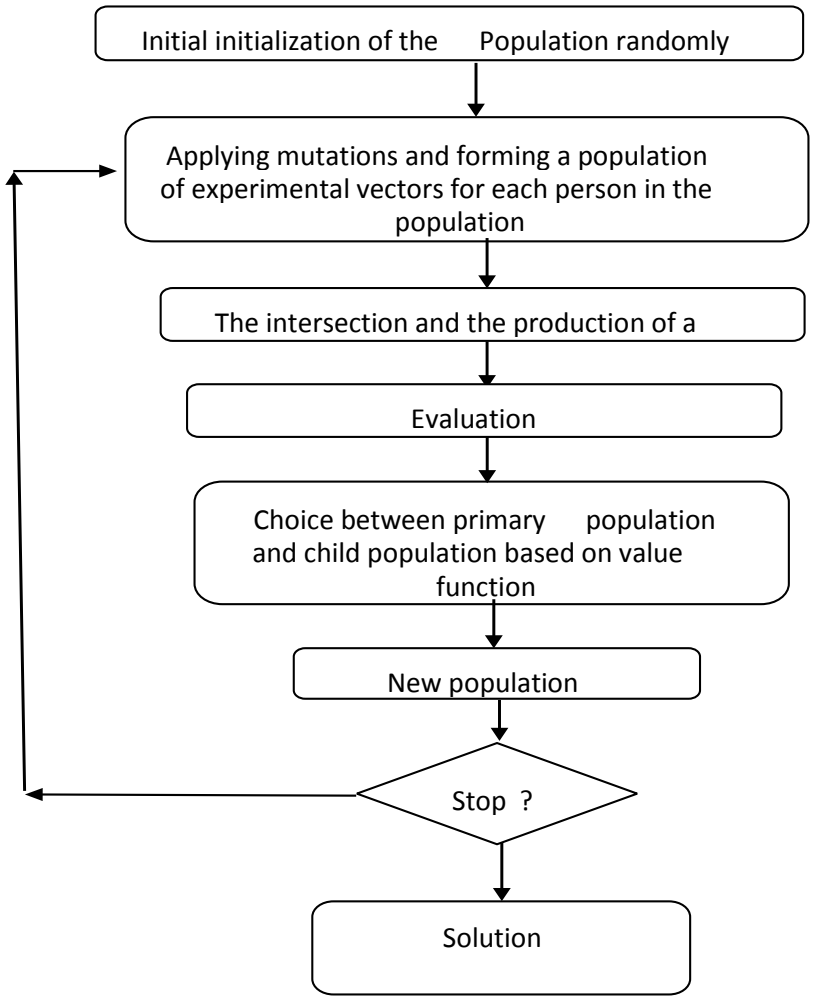

Figure 2. Flowchart of differential evolution algorithm

4. DATA ANALYSIS METHOD

The differential evolution algorithm is implemented using MATLAB software. However, the simulation results can be derived using precise transistor models in the H-Spice software. The values of the parameters are determined by using the differential evolution algorithm called in the H-Spice input file by MATLAB. Finally, values of output parameters of voltage gain, bandwidth, phase margin, power consumption and chip level are calculated and then can be detected for each member.

5. SIMULATION RESULTS

After running 150 generations, the number of the population reached 1653 which the cost functions values of population members are two by two have been drawn in Figures 3 -5, indicates the proper dispersion of the algorithm.

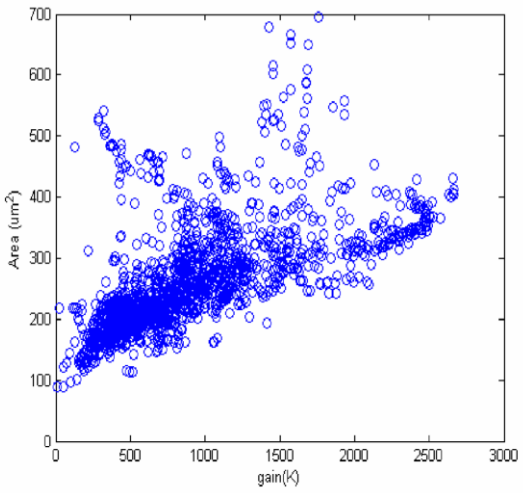

Figure 3. The contrast between the gain and the chip level of the population member

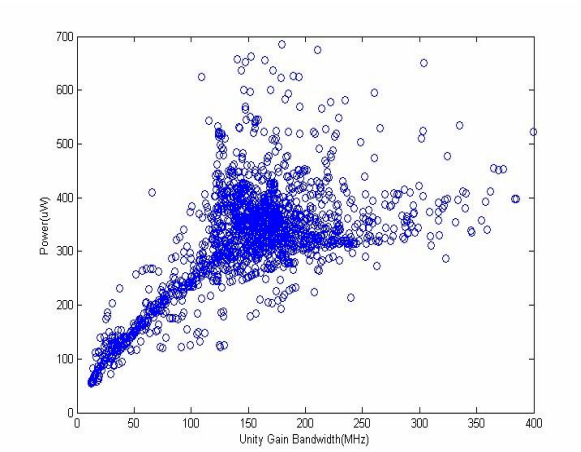

Figure 4. conflict between bandwidth and power consumption of population members

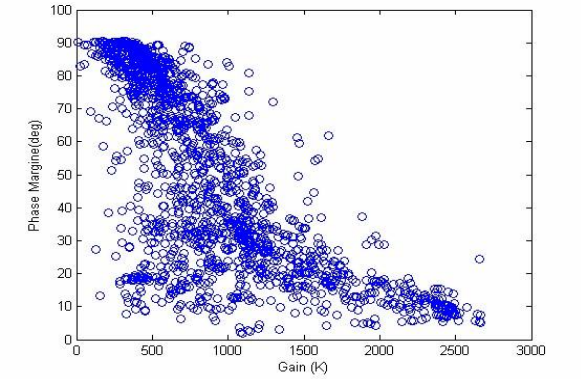

Figure 5. The rate of conflict between the gain and the phase margin of the population members

As can be seen, higher gain responses occupy a higher level (Figure 3 and high bandwidth responses take more power (Figure 4). Additionally, the margin of the phase decreases with increasing gain (Figure. 5). The implementation time of algorithm is depended on the number of Hspice performances and lasted about 1.5 hours, in which case only an AC analysis took place that takes a little time. Among the members of the population, those answers present as an initial set of answers, in which 297 are acceptable results. Among the acceptable answers, firstly, with analyzing the transient state (which requires more time), the answers which have desired conditions in terms of the maximum output voltage range, and then with analyzing all the processing corners and temperatures, the answers which have the least favorable conditions in all corners introduced as the final answer set. Table 4 shows a comparison of results of manual calculation and many answers of differential evolution algorithm.

Table 1. Comparison of manual computational results with many answers of differential evolution algorithm

Parameter	Manual calculations values	DE (1)	DE (2)	DE (3)
W/L (M1)	20u/0.5u	43u/0.28u	60.5u/0.46u	41.5u/0.36u
W/L (M2)	20u/0.5u	43u/0.28u	60.5u/0.46u	41.5u/0.36u
W/L (M3)	5u/0.5u	8.4u/0.44u	14.3u/0.53u	16.5u/0.37u
W/L (M4)	5u/0.5u	8.4u/0.44u	14.3u/0.53u	16.5u/0.37u
W/L (M5)	5u/0.5u	17.4u/0.46u	5.5u/0.44u	10.8u/0.37u
W/L (M6)	5u/0.5u	17.4u/0.46u	5.5u/0.44u	10.8u/0.37u
W/L (M7)	10u/1u	22.4u/0.75u	9.5u/0.56u	19.4u/0.63u
W/L (M8)	10u/1u	22.4u/0.75u	9.5u/0.56u	19.4u/0.63u
W/L (M9)	5.5u/0.5u	11.6u/0.5u	6.2u/0.5u	13.3u/0.5u
W/L (M10)	15u/0.3u	17.4u/0.51u	8.6u/0.62u	21.6u/0.59u
W/L (M11)	6u/0.5u	91.5u/1.39u	47.8u/1.36u	90.4u/1.2u
VG3	0.74 V	0.82 V	0.8 V	0.8 V
VG5	0.74 V	0.85 V	0.85 V	0.86 V
VCM(IN)	1.4 V	1.56 V	1.57 V	1.54 V
C_C (PF)	390	395.5	337	364.5
Gain (K)	167	410	668	381
Bandwidth (MHz)	112.13	156.13	364	166
Phase margin	83 ◦	87 ◦	77 ◦	86 ◦
Power	253.8	389.9	454	439
consumption (μW)				
Chip level (μm^2)	212	198	269	187

6. CONCLUSION

In this research, multi-objective differential evolution algorithm was used to design and optimize the amplifier. The simulation results proved that the resulting algorithm could optimize such a circuit from a different point of view. As could be seen, the set of answers obtained from the differential evolution algorithm had a higher quality and variety than the result of manual calculations. In terms of time required for design, the manual calculation method was much longer than the differential evolution algorithm. This was due to the need to adjust the initial values of the elements with a large amount of effort and error, which was very timely in the manual calculation method for achieving optimal quality, since at each stage the designer only changed one of the input parameters, then simulation was performed and the results were analyzed. Another reason of time-consuming manual design is the contrast between the output parameters, so that the improvement of a parameter would weaken other parameters. On the other hand, , the integrated circuit designers by manual calculations due to several limitations through choosing parameters cannot verify the results while by using differential evolution algorithm the designers are always satisfy the results which it is the best solution.

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