DESIGN OF ASYMMETRICAL BOOST CONVERTERS BASED ON PHOTOVOLTAIC SYSTEMS REQUIREMENTS

DISEÑO DE CONVERTIDORES ELEVADORES ASIMÉTRICOS PARA APLICACIONES FOTOVOLTAICAS

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ABSTRACT: An asymmetrical interleaved dual boost DC/DC switching converter is proposed to improve photovoltaic systems. Such a new step-up power converter provides a low input current ripple injected into the photovoltaic generator, and at the same time provides a low voltage ripple to the load. The developed converter is based on traditional interleaved boost converters interacting with voltage multiplier cells where the circuit symmetry has been broken, obtaining an inherent discontinuous conduction-operating mode that provides a high voltage conversion ratio in comparison to traditional solutions. Such low-ripple and high boosting conditions make this converter an ideal candidate for photovoltaic systems design, in particular for grid-connected applications. The converter circuitry is analyzed, and a design procedure is proposed in terms of typical photovoltaic systems requirements, providing simple but useful equations. Finally, the converter design is illustrated by means of a realistic design example and validated by using an experimental prototype.

KEYWORDS: photovoltaic systems, DC/DC switching converters, asymmetrical interleaved, discontinuous conduction mode

RESUMEN: Este artículo presenta un convertidor conmutado DC/DC elevador, entrelazado y asimétrico, propuesto para interactuar con sistemas fotovoltaicos. Este nuevo convertidor provee condiciones de bajo-rizado de corriente al generador fotovoltaico y de bajo-rizado de voltaje a la carga. Así mismo, el convertidor está basado en estructuras entrelazadas típicas interactuando con celdas multiplicadoras de voltaje, donde la simetría del circuito se rompe para obtener un convertidor que opera inherentemente en modo de conducción discontinuo que provee una razón de elevación de tensión superior a las soluciones tradicionales. Las características de bajo rizado y alta elevación hacen de este convertidor un candidato ideal para interactuar con sistemas fotovoltaicos, y en particular con sistemas conectados a la red eléctrica. El convertidor es analizado circuitalmente, y se propone un procedimiento de diseño basado en requerimientos típicos de los sistemas fotovoltaicos, presentando ecuaciones de diseño simples pero útiles. Finalmente, el diseño del convertidor se ilustra a través de un ejemplo de diseño realista, y se valida usando un prototipo experimental.

PALABRAS CLAVE: sistemas fotovoltaicos, conversores DC/DC conmutados, entrelazado asimétrico, modo de conducción discontinuo

1. INTRODUCTION

Photovoltaic power systems are efficient alternatives to provide electrical energy providing redundancy for critical applications, *in situ* energy generation [1], and the reduction of traditional energy generation that impacts the environment. Similarly, photovoltaic generators have been intensively used in residential applications [2–4], and autonomous and portable applications [5].

Photovoltaic systems require a power electronics interface to define their operating point at optimal conditions for any load or grid-connection. This aspect has been addressed by single-stage inverters [6], or by adopting double-stage structures based on DC/DC and DC/AC converters [7]. The double-stage approach is widely accepted due to its application in distributed generation system based on multiple generators [2], as well as in stand-alone DC applications, where a single DC/DC converter is required [4].

The PV applications commonly adopt boosting converters for grid-connected applications due to the requirement of increasing the voltage to the grid-connected inverter operating conditions. The most commonly used DC/DC converter in the first stage of such systems is the classical boost converter [2,7], which provides an acceptable voltage conversion ratio, and also requests a continuous current from the photovoltaic (PV) panel. Other characteristics required in PV applications are a low current ripple injected to the PV and high conversion efficiency. The current ripple magnitude is an important factor in the selection of power converters for PV applications because high current ripples produce an oscillation around the maximum power point (MPP) [8,9] that reduces the energy extracted from the PV generator.

The boost converter is a good candidate for interfacing PV systems among other converters [2,7]. But in such a boost converter, the current ripples injected to the PV generators depend on the inductor size, switching frequency, input capacitor, and high frequency power source impedance; therefore, in order to reduce the current ripple, it is necessary to increase the converter inductance or input capacitance, modifying the dynamics of the system. This can be addressed by using an additional filter between the PV generator and the power converter, also increasing power losses, size, weight, cost, and the order of the system. Another possibility for reducing the converter's input current ripple is given by the interleaving structures [10], which considers the connection of DC/DC converters in parallel to share the power flow between two or more branches. This implies a reduction in the size, weight, and volume of the inductors and capacitors [11]. In addition, a proper control of the parallel converters increases the ripple frequency and reduces the ripple waveforms at the input and output of the power conversion system [12], which leads to a significant reduction of the current and voltage ripples. The interleaving solution has been successfully adopted in photovoltaic applications [8], but traditional interleaving structures require current control loops in each phase to ensure proper current sharing among the parallelized converters, since differences in the phase impedances causes imbalances in the phase currents.

To achieve a high voltage conversion ratio, it is possible to use voltage multiplier cells to increase the traditional

DC/DC converters voltage conversion ratio [13]. This solution impacts the behavior of the original power converter and the resulting circuit can be operated in continuous (CCM) or discontinuous (DCM) conduction mode. In PV systems, power converters can be operated in both CCM [2,9] and DCM [6], depending on the power converter design.

This paper proposes an asymmetrical interleaved dual boost converter (AIDB) topology and design procedure for photovoltaic power systems. The AIDB has been developed from the traditional interleaved boost converter interacting with voltage multiplier cells to provide higher conversion ratio compared with the traditional structure, but preserving the characteristic of small input current and output voltage ripples. In addition, the AIDB does not require internal current control loops to ensure current sharing among the parallelized converters [12], which reduces the complexity of the overall control system.

Moreover, the AIDB exhibits an inherent DCM operation, which in traditional and interleaved DC/DC converters [14,15], implies a dependency of the voltage conversion ratio from the circuit parameters and load impedance, making it difficult to design for non-constant load conditions. In contrast, the AIDB voltage conversion ratio does not depend on the circuit or load parameters.

The remaining part of the paper is organized as follows: in Section 2 the AIDB converter circuital analysis is performed and a design process for PV applications is proposed. Then, Section 3 illustrates the AIDB topology and design by means of an application example experimentally validated. Finally, the conclusions are given in Section 4.

2. ASYMMETRICAL INTERLEAVED DUAL BOOST ANALYSIS AND DESIGN

The interleaving technique consists in the parallel interconnection of a determined number of identical converters, in which control signals are strategically phase shifted in each switching period. This arrangement reduces the net ripple amplitude through harmonic cancellation and raises the effective ripple frequency of the overall converter without increasing switching losses or device stresses, and divides the input power between the branches. An interleaved system reduces the ripple filtering

requirements, the conduction losses, and prototype size without sacrificing conversion efficiency [10].

In the interleaved interconnection of two switching converters, the ripples can be significantly reduced by using two optimal configurations: when one switch is ON at the same time that the other one is OFF. In these optimal configurations, the inductor current of one converter is increasing while the other inductor current is decreasing, therefore the inductor current waveforms of the two converters have slopes with opposite signs, while the slope of the total interleaved input current is reduced, as well as its ripple. Consequently, if the aim is to obtain low input and output ripples, the interleaved circuit has to be controlled to turn on the switches in a complementary way. This complementary interleaving offers more simplicity in the control design than other kinds of interleaving, because one activation signal is the opposite of the other activation signal [11].
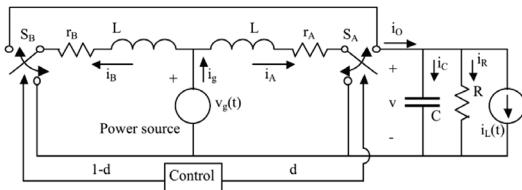
Figure 1. IDB circuital scheme.
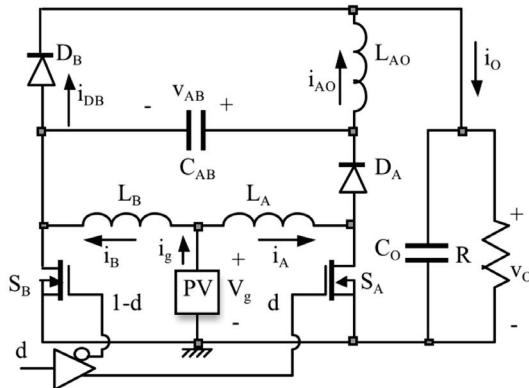
Figure 2. AIDB circuital scheme

The asymmetrical interleaved dual boost or AIDB, was obtained from the traditional interleaved dual boost (IDB) converter [8]—whose circuital scheme is given in Fig.1—by connecting a voltage multiplier cell [13] at its output port. Then, the order of the output filter was increased to reduce the output voltage ripple, done by introducing inductive filters at the branch outputs.

Such a structure exhibits a similar behavior to the IDB [11], where the CCM operating condition is constrained to duty cycles near to 0.5; therefore, it is not possible to regulate it. To avoid this limitation, the symmetry of the structure is broken, obtaining the asymmetrical circuit depicted in Fig. 2, where, in addition, the power source is now a PV panel.

The AIDB is basically a parallel interconnection between a boost converter with an output filter (branch A) and a traditional boost converter (branch B) in which the first capacitor of the A-branch output filter is connected to the intermediate node of the boost of the B-branch. This method follows the concept of switching capacitor-based voltage multiplier cells. The MOSFETs SA and SB are activated in a complementary way to obtain the desired input current ripple reduction.

2.1 Circuit analysis and topologies

In the following, lowercase letters refer to dynamic variables and uppercase letters refer to steady-state variables.

The sequence of operation intervals, which have the respective duration of d_1T, d_2T, and d_3T, can be defined using Fig. 3 which shows the DCM currents in the AIDB circuit, without loss of generality, for a duty cycle of 50%. The definition of the operation intervals is the following:

$$d_1 + d_2 + d_3 = 1 \tag{1}$$

$$d_1 = 1 - d = d'; \quad d_2 + d_3 = d \tag{2}$$

Figure 4 shows the topologies of the converter in each operation interval. The topologies were identified using both the simulation waveforms and the usual procedure of assuming all the possible positions in the switches. The states of the switches in the four topologies are defined as:

- Topology 1: S_B and D_A ON; S_A and D_B OFF. Interval 1: d' = d_1

- Topology 2: S_A and D_B ON; S_B and D_A OFF. Interval 2: d_2

- Topology 3: S_A ON; S_B, D_A and D_B OFF, where D_B is in DCM. Interval 3: d_3
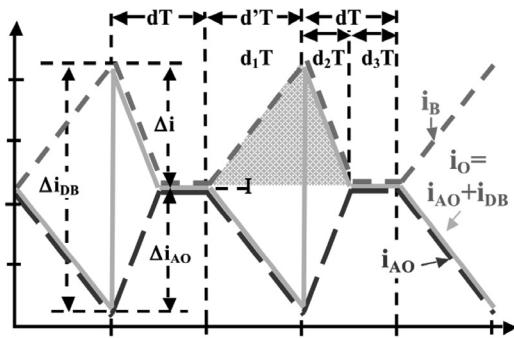
Figure 3. AIDB operation intervals

a) Topology 1. Interval 1: d' = d₁

b) Topology 2. Interval 2: d₂

c) Topology 3. Interval 3 (D_B DCM): d₃

d) Topology 4. (D_A DCM)
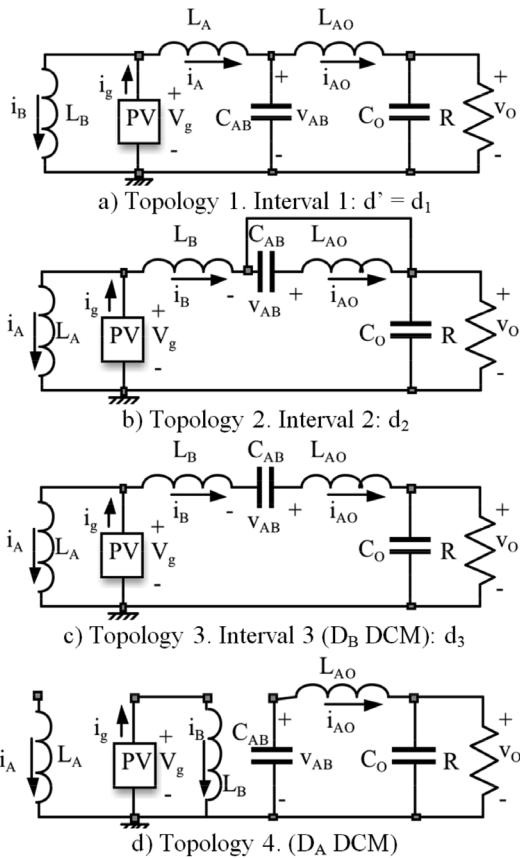
Figure 4. AIDB topologies

- Topology 4: S_B ON; S_A, D_A and D_B OFF, where D_A is in DCM

Depending on the duty cycle, two operation sequences may occur: For duty cycles greater than 0.382, the converter structure follows topologies 1, 2, and 3; while for duty cycles lower than 0.382, the converter structure changes into topologies 1, 4, and 2. In the first sequence, which is the one for the desired operation, the transition

from topology 1 to topology 2 occurs by the change of the MOSFET states. The transition from topology 2 to topology 3 takes place when i_B and i_{AO} are equal, therefore the diode D_B current becomes zero. Finally, the transition from topology 3 to topology 1 is driven by the change of the MOSFET states. Similarly, in the second sequence, which is a not the desired one, the transition from topology 1 to topology 4 occurs when i_A current becomes zero. The transitions from topology 4 to topology 2 and from topology 2 to topology 1 are driven by the change of the MOSFET states.

The operation sequence 1-2-3 provides low input current and output voltage ripples, which are required for photovoltaic systems. The low ripple conditions are due to the continuous waveform of the L_A inductor current, therefore it produces a low harmonic content. On the contrary, sequence 1-4-2 forces both L_A and L_B discontinuous inductor currents producing a high harmonic content.

From the AIDB topologies depicted in Fig. 4, a permanent loop is found: voltage source V_g, inductors L_B and L_{AO}, and capacitors C_{AB} and C_O. Considering the converter in steady-state [14], Eq. (3) can be obtained from the permanent loop, where V_{AB} represents the C_{AB} voltage, V_g the input voltage, and V_O the output voltage.

$$V_g + V_{AB} - V_O = 0 \tag{3}$$

Similarly, from the amplitude of the L_A current ripple on the first and second or third topologies, the expressions for steady-state V_{AB} and output voltage V_O are given by (4) and (5), respectively.

$$V_{AB} - V_g / D' = 0 \tag{4}$$

$$V_O = V_g (2 - D) / D' \tag{5}$$

where the voltage conversion ratio for the AIDB converter is given by (6), which is higher than the one provided by the traditional boost converter (7) [14] for the same duty cycle.

$$\frac{V_O}{V_g} = \frac{2 - D}{1 - D} \text{, for the AIDB converter} \tag{6}$$

$$\frac{V_O}{V_g} = \frac{1}{1 - D} \text{, for the boost converter} \tag{7}$$

Analyzing the permanent loop in topology 3, it is

found that the voltages on L_B and L_{AO} have an equal magnitude but the opposite sign (8), while L_B and L_{AO} are series, therefore their currents are equal (9). Then, deriving (9), the relation given by (10) is found.

$$V_{LB} = V_{LAO} \tag{8}$$

$$i_B = i_{AO} \tag{9}$$

$$L_{AO} \cdot V_{LB} = L_B \cdot V_{LAO} \tag{10}$$

The solution for the equation system (8–10) is $V_{LB} = V_{LAO} = 0$, which implies that i_B and i_{AO} are equal and constant in the interval $D_3 T$.

From the ripple amplitude of the L_B current in the first and second topologies, taking into account the output voltage magnitude (5) and intervals duration relations (1–2), D_2, and D_3 are given by:

$$D_2 = (1-D)^2 \tag{11}$$

$$D_3 = 1 - D' - (D')^2 \tag{12}$$

It is noted that the AIDB intervals duration and voltage conversion ratio do not depend on the converters or load parameters despite their DCM operation. This is an improvement over classical converters such as boost, buck, or buck-boost.

From (12) it is found that $D = 0.382$ defines an operation limit for the converter, because $0 < D < 0.382$ imply $D_3 < 0$, therefore the AIDB is not operating in the desired sequence 1-2-3.

The average current in C_{AB} in the first, second, and third topologies is given by I_A-I_{AO}, -I_{AO}, and -I_{AO} = -I_B, respectively, where capitol letters corresponds to the steady state currents of L_A, L_{AO}, and L_B. From the charge balance on C_{AB} and taking into account that $D_2 + D_3 = D$ as given in (2), the relation between I_A and I_{AO} is given by $I_A = I_{AO}/D'$. Similarly, from the steady state charge balance on the output capacitor C_O, taking into account that in topologies 2 and 3 the average output current is supplied exclusively by L_B, from the series connection of L_B and L_{AO} in the third topology, and from the D_2 and D_3 length (11–12), the relation between I_{AO} and I_B is $I_{AO} = I_B$. From the previous analyses and the AIDB voltage conversion ratio, the AIDB steady state

inductors currents are:

$$I_A = \frac{I_{AO}}{(1-D)} \tag{13}$$

$$I_B = I_{AO} = \frac{V_g(2-D)}{R(1-D)} \tag{14}$$

Equation (14) shows that the current sharing among L_A and L_{AO} is naturally defined by the AIDB structure without any additional control loops, and Eq. (13) gives information about the inductor current ratings, where it is noted that L_A inductor must be heavier and bulkier than L_{AO} and L_B.

2.2 Design procedure and equations

The proposed AIDB design process is intended to fulfill typical requirements in photovoltaic systems. The aspect imposed is the voltage conversion ratio since PV generators define the AIDB input voltage, while the load specifications define the converter output voltage; i.e., grid connected inverter. The steady state duty cycle for given input and output voltages is:

$$D = \frac{1}{1 - V_g/V_O} - \frac{2}{V_O/V_g - 1} \tag{15}$$

The input current ripple amplitude is another important condition to be designed. In this way, the amplitude of the AIDB input current ripple corresponds to the magnitude difference between L_A and L_B current ripples, which in topologies 1, 2, and 3, are given by (16), (17), and (18), respectively.

$$\Phi_1 = V_g T \left[\frac{1-D}{L_B} - \frac{D}{L_A} \right] \tag{16}$$

$$\Phi_2 = V_g T \left[\frac{(1-D)^2}{L_A} - \frac{(1-D)}{L_B} \right] \tag{17}$$

$$\Phi_3 = V_g T \left[\frac{1 - (1-D) - (1-D)^2}{L_A} \right] \tag{18}$$

Taking into account that the converter steady-state condition, $\Phi_1 + \Phi_2 + \Phi_3 = 0$, which implies that the magnitude of the larger ripple section must be equal to the sum of the magnitudes of the other ones. Adopting the design condition $L_A = L_B = L$, it is noted that $\Phi_1 <$

Φ_2 for $0.382 < D < 1$, $\Phi_1 < \Phi_3$ for $0.439 < D < 1$, and $\Phi_2 < \Phi_3$ for $0.5 < D < 1$. Such relations allow for one to define a design equation for L_A and L_B as

$$L_A = L_B = L \tag{19}$$

$$L = \frac{V_g T(1-D)D}{\Phi}, for\ 0.382 < D < 0.5 \tag{20}$$

$$L = \frac{V_g T\left[1-D'-(D')^2\right]}{\Phi}, for\ 0.5 < D < 1 \tag{21}$$

where Φ represents the desired input current ripple magnitude. Similarly, L_{AO} inductor can be designed in agreement with the desired inductor current ripple Φ_{AO} as
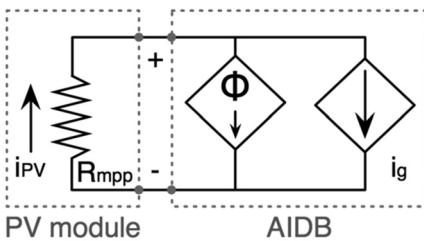
Figure 5. PV-AIDB connection: small signal model

$$L_{AO} = \frac{T\left[V_g - V_O(1-D)\right]}{\Phi_{AO}} \tag{22}$$

In addition, $L_{AO} = L_B$ condition provides a triangular waveform of the C_{AB} voltage, which is a convenient condition for classical control-oriented modeling approaches [14].

Moreover, the input current ripple magnitude Φ will impact the power produced by the PV module since it generates an undesired oscillation around the desired operating point. To analyze this effect, the small signal equivalent circuit of the PV module-AIDB converter is depicted in Fig. 5, where the AIDB input current, in steady-state, can be modeled by $i_g(t) = \Phi(t) + I_g(t)$. $\Phi(t)$ represents the small-signal oscillation and $I_g(t)$ the steady-state current. In the model, $R_{mpp} = V_{mpp}/I_{mpp}$ represents the small-signal behavior of the PV module [16] named *PV module differential resistance*, while V_{mpp} and I_{mpp} are the PV voltage and current at the maximum power point (MPP). Since a PV generator exhibits an optimal operating condition or MPP, a control algorithm to track such a condition, named the *maximum power point tracking* (MPPT) controller, is necessary.

Taking into account that a properly designed MPPT controller provides an MPPT efficiency higher than 99% [16], the oscillation on the power due to the AIDB input current ripple must be lower than 0.1% to avoid sensible additional losses; therefore, the current ripple magnitude that generates such a maximum desired power oscillation Φ_P can be approximated by

$$\Phi_P / P_{mpp} = 0.1\% \tag{23}$$

$$\Phi_P = R_{mpp}\Phi^2 \tag{24}$$

where P_{mpp} represents the PV power and the MPP.

The C_{AB} capacitor design must be performed in order to guarantee a maximum allowed capacitor voltage ripple Φ_{AB} to avoid damages in transient conditions. Equation (25) gives the C_{AB} value that ensures a maximum Φ_{AB} for a desired load impedance R, duty cycle D, and C_{AB} steady state voltage V_{AB}.

$$C_{AB} = \frac{V_{AB}T(2-D)D}{\Phi_{AB}R} \tag{25}$$

The design of the output capacitor C_O is performed to fulfill a given output voltage ripple requirement Φ_O. From the second order filter analysis given in [14], Eq. (26) provides the C_O value to for a given duty cycle and L_{AO} conditions.

$$C_O = \frac{V_g T^2(1-D)^2}{2L_{AO}\Phi_O} \tag{26}$$

3. APPLICATION EXAMPLE

This AIDB design example considers a grid connected PV application that requires a step-up condition to meet the inverter stage input voltage level [6]. In addition, a PV panel Sharp NU-U235F1 is considered, which consists of three cell-strings in series, each one of them equipped with a by-pass diode [16]. Consequently, the NU-U235F1 is composed by three PV modules, each one of them exhibiting $P_{mpp} = 78$ W, $V_{mpp} = 10$ V, $I_{mpp} = 7.84$ A, open circuit voltage $V_{oc} = 12.33$ V, and short-circuit current $I_{sc} = 8.60$ A, all of those parameters are measured under standard test conditions (STC). The current-voltage (I-V) and power-voltage (P-V) characteristic curves for a single PV module of such a commercial PV panel are depicted in Fig. 6, where 1000 W/m², 800 W/m², and 600 W/m² irradiance conditions are illustrated.

For a typical 500 W and 120 VAC grid-connected full-bridge inverter, the PV system requires two NU-U235F1 PV panels that correspond to 95% of the maximum inverter power. The full-bridge inverter requires approximately 170 VDC to meet the desired grid voltage, and to provide an additional 5% of safe margin to compensate for parasitic losses, this example considers the input voltage of the inverter equal to 180 V. Such a condition defines the AIDB input and output voltages $V_g = 10$ V and $V_O = 30$ V, respectively; therefore, the duty cycle in the MPPT conditions is $D = 0.5$ as given in (15). It is noted that a 500 W PV system with two NU-U235F1 PV panels requires 6 AIDB converters, one for each PV module, all of them identical. Therefore, this example presents the design and experimental validation of a single converter.

For the considered NU-U235F1 PV modules, $R_{mpp} = 1.276$ Ω, $\Phi_P = 78$ mW, and $\Phi = 247.3$ mA. In addition, the switching frequency was selected as $f_{sw} = 50$ kHz; therefore, the switching period T = 20 µs. From Eqs. (19–21), the input inductors are calculated to be equal to 202.18 µH, where near commercial inductors $L_A = L_B = 200$ µH were found. Similarly, to obtain a C_{AB} triangular voltage waveform, $L_{AO} = L_B = 200$ µH was adopted.

In the same way, C_{AB} and C_O have been designed to achieve small voltage ripples using Eqs. (25) and (26), respectively. In this example, $\Phi_{AB} = 3\%$ and $\Phi_O = 0.4\%$ have been defined, but it is noted that any other requirements can be imposed. From such conditions, $C_{AB} = 50$ µF and $C_O = 20.83$ µF, where the capacitances achievable with commercially available capacitors were $C_{AB} = 50$ µF with five 10 µF capacitors, and $C_O = 23.5$ µF with five 4.7 µF capacitors.

The AIDB experimental prototype has been implemented as depicted in Fig. 7(a), where the three inductors and two capacitors banks are observed. In such an experimental prototype, the measured series resistances in L_A, L_B, and L_{AO} were $R_{LA} = 34$ mΩ and $R_{LB} = R_{LAO} = 66$ mΩ, respectively. Similarly, the series resistances in C_{AB} and C_O were $R_{CAB} = R_{CO} = 81$ µΩ, the MOSFETs and DIODEs used were IRFP054 and MBR1045, respectively, and a complementary output IR4428 driver was used to manage both MOSFETs. Figure 7(b) shows the laboratory set-up used to perform the experimental measurements, which validate the AIDB design procedure and equations.

The operating conditions of the AIDB experimental prototype have been defined in agreement with the design example requirements: 10 V input voltage and 7.68 input current, duty cycle equal to 50%, and a 30 V load voltage. Figure 8(a) shows the experimental L_B and L_{AO} currents, where the AIDB inherent DCM operating condition is exhibited, validating the Fig. 3 analyses since both figures are in agreement, and illustrating the three operating intervals d_1, d_2, and d_3, which additionally puts the operation in the sequence 1-2-3 in evidence.

Figure 8(b) depicts the experimental AIDB input current waveform, where the small input current ripple condition imposed in the design process is achieved. The current ripple has been measured by using a current-to-voltage sensor with a gain equal to 25 mV/mA, reporting $\Phi = 255$ mA that corresponds to an error of 3% over the designed value. Similarly, Fig. 8(c) presents the experimental output voltage ripple, whose amplitude is in agreement with the design example calculation given by Eq. (26), exhibiting an error of 6% over the theoretical prediction. Moreover, Fig. 8(d) presents the efficiency of the experimental prototype for duty cycle conditions within $0.382 < D < 0.660$, which at the particular design operating point (D = 0.5) is equal to 89.74%. It is noted that the experimental duty cycle range must be limited to $D > 0.382$ in order to guarantee the AIDB operation in the low-ripple sequence 1-2-3.

Finally, the experimental results exhibit a satisfactory agreement with the design calculations, validating the proposed design process.
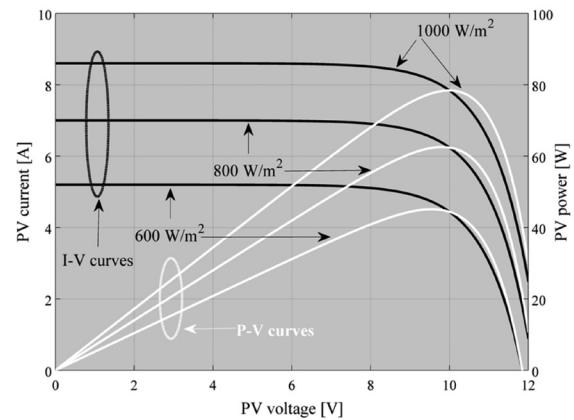
Figure 6. I-V and P-V curves for the Sharp NU-U235F1: single module

(a) Experimental prototype   **(b)** Laboratory set-up
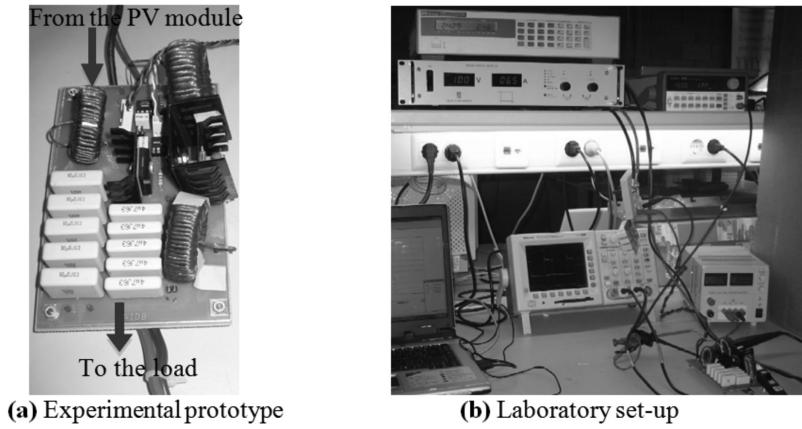
Figure 7. AIDB experimental test bench

(a) Discontinuous currents I_{AO} and I_B for D = 0.5

(b) Input current ripple for D = 0.5

(c) Output voltage ripple for D = 0.5

(b) Efficiency
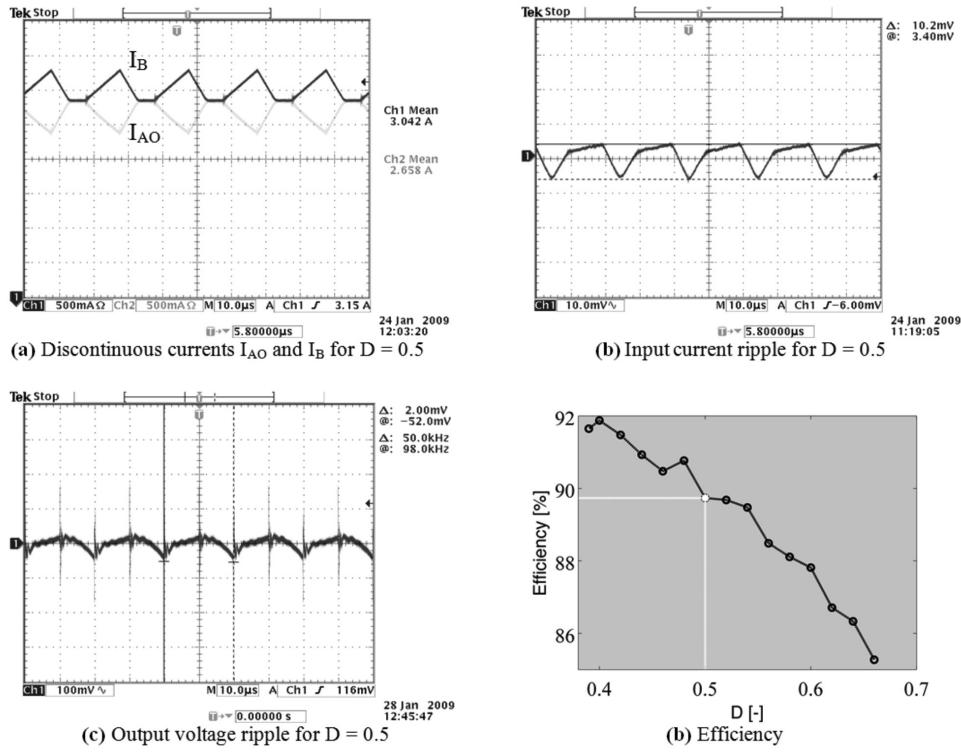
Figure 8. AIDB experimental measurements

4. CONCLUSIONS

An asymmetrical interleaved dual boost converter designed to interact with photovoltaic systems has been proposed, analyzed, and experimentally validated. The converter was developed by breaking the symmetry of traditional interleaved boost converters with voltage multiplier cells.

The proposed AIDB converter provides reduced input current and output voltage ripples for duty cycles higher than 0.382, while in other conditions the converter operates in an undesired and non-optimal topologies sequence. Moreover, the AIDB exhibits an inherent DCM condition that causes a natural current sharing among the parallelized branches without any additional current controller, while its voltage conversion ratio does not depend on converter or load parameters like in conventional DCM converters,

which will simplify a regulation strategy design for the AIDB converter. Moreover, the AIDB small input current and output voltage ripple conditions avoid power losses due to oscillations around the PV panel MPP, and at the same time provide a high quality power supply to the load by avoiding undesired current and voltage harmonics.

The AIDB design process has also been proposed, which is based on typical photovoltaic systems requirements. Such a design procedure has been illustrated and experimentally validated by means of laboratory tests on a real AIDB prototype. The measurements show a satisfactory agreement with the theoretical predictions.

Finally, the operation of the AIDB converter can be improved by adopting non-linear control strategies, like the one proposed in [17], to reject environmental or load perturbations.

ACKNOWLEDGEMENTS

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